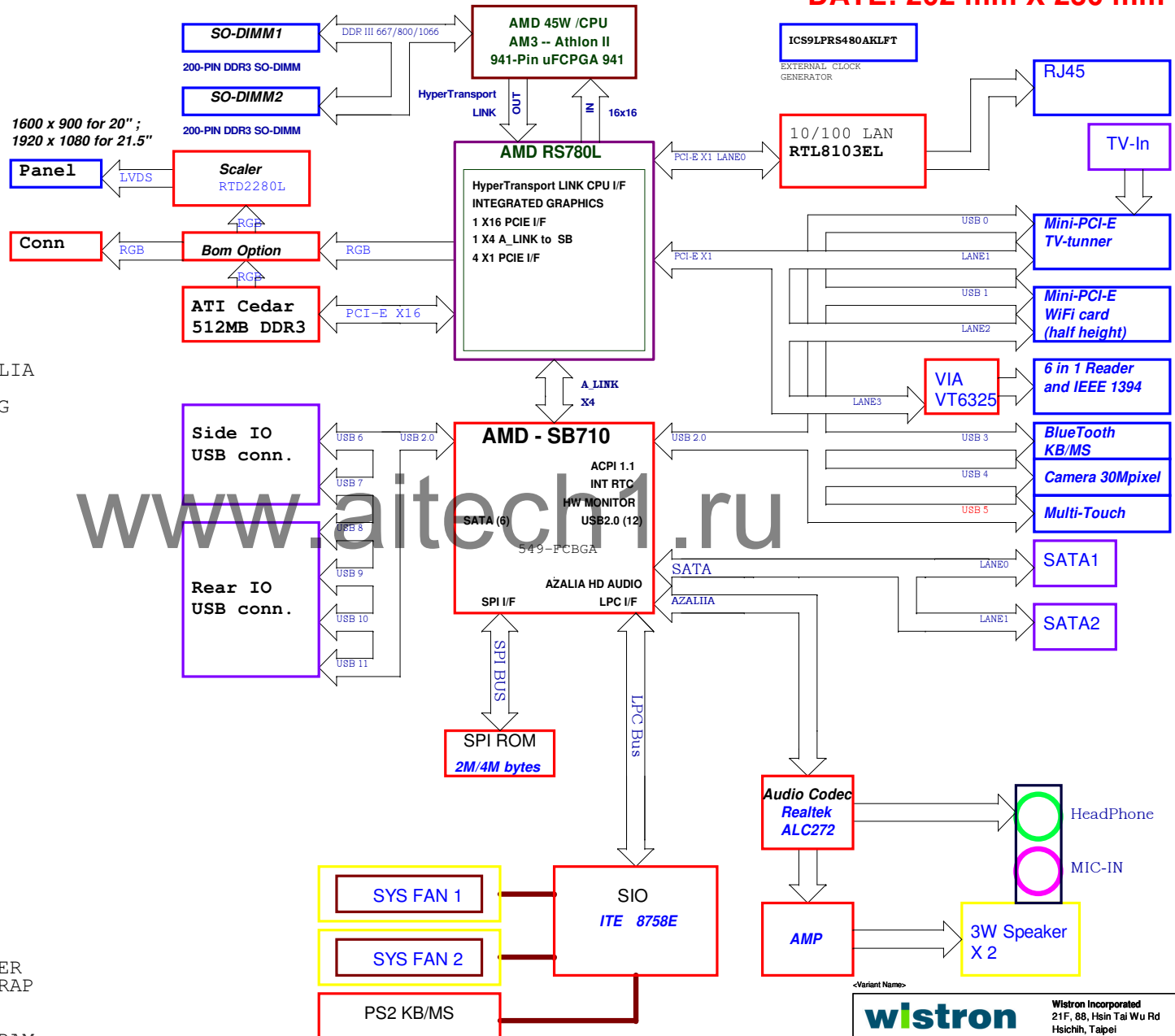


## SHEET

Sheet 1 COVER PAGE  
Sheet 2 POWER DELIVERY CHART  
Sheet 3 Clock MAP  
Sheet 4 RESET & POWER MAP  
Sheet 5 PWR Sequence and PCIRST#  
Sheet 6 GPIO table  
Sheet 7 FAN/Screw Holes  
Sheet 8 EXTERNAL CLOCK GENERATOR  
Sheet 9 CPU HT INTERFACE  
Sheet 10 CPU CNTL/STRAPS  
Sheet 11 CPU MEM\_A  
Sheet 12 CPU MEM\_B  
Sheet 13 CPU POWER/GND  
Sheet 14 CPU DECOUPLING  
Sheet 15 RS780L-HT LINK0 I/F  
Sheet 16 RS780L-PCIE LINK I/F  
Sheet 17 RS780L-SYSTEM I/F & DDC  
Sheet 18 RS780L-POWER  
Sheet 19 NB 5th (Reserved)  
Sheet 20 NB 6th (Reserved)  
Sheet 21 DDRIII-DIMM SLOT  
Sheet 22 MEM Terms & Deaps  
Sheet 23 SB710-PCIE/PCI/CPU/LPC  
Sheet 24 SB710-ACPI/GPIO/USB/AZALIA  
Sheet 25 SB710-SATA/IDE  
Sheet 26 SB710-POWER & DECOUPLING  
Sheet 27 SB710-STRAPS  
Sheet 28 LVDS RTD22x0  
Sheet 29 AUDIO CODEC ALC272  
Sheet 30 Mini PCIE Slot  
Sheet 31 VGA Switch  
Sheet 32 SATA Connector  
Sheet 33 Rear USBX4 Conn  
Sheet 34 Side USBx2 +RJ45  
Sheet 35 VT6325 1394/CARD READER  
Sheet 36 USB device  
Sheet 37 PS2 KB/MS CONN  
Sheet 38 AMP  
Sheet 39 Fast 10/100 LAN RTL8103  
Sheet 40 HP/Mic Jack  
Sheet 41 ITE 8758E  
Sheet 42 Key\_Pad/LED/PWRBTN  
Sheet 43 ADAPTER/PCIRST/SPI  
Sheet 44 NCP1589 +12V\_S0  
Sheet 45 RT8205A\_3V&5V\_EuP  
Sheet 46 Run Time Power  
Sheet 47 Chipset Core Power  
Sheet 48 DDR & Termination Power  
Sheet 49 LDO & Other PWM  
Sheet 50 VCORE\_NCP5393 (1)  
Sheet 51 VCORE\_NCP5393 (2)  
Sheet 52 RT8209E\_1D5V\_VRAM  
Sheet 53 RT8208\_VGA\_CORE  
Sheet 54 Cedar ( 1 of 5 ) PCIE  
Sheet 55 Cedar ( 2 of 5 ) IO  
Sheet 56 Cedar ( 3 of 5 ) POWER  
Sheet 57 Cedar ( 4 of 5 ) DP POWER  
Sheet 58 Cedar ( 5 of 5 ) MEM/STRAP  
Sheet 59 VRAM Rank1  
Sheet 60 VRAM Rank2 (Reserve)  
Sheet 61 GPU POWER SEQUENCE DIAGRAM  
Sheet 62 CTF/PPLAY

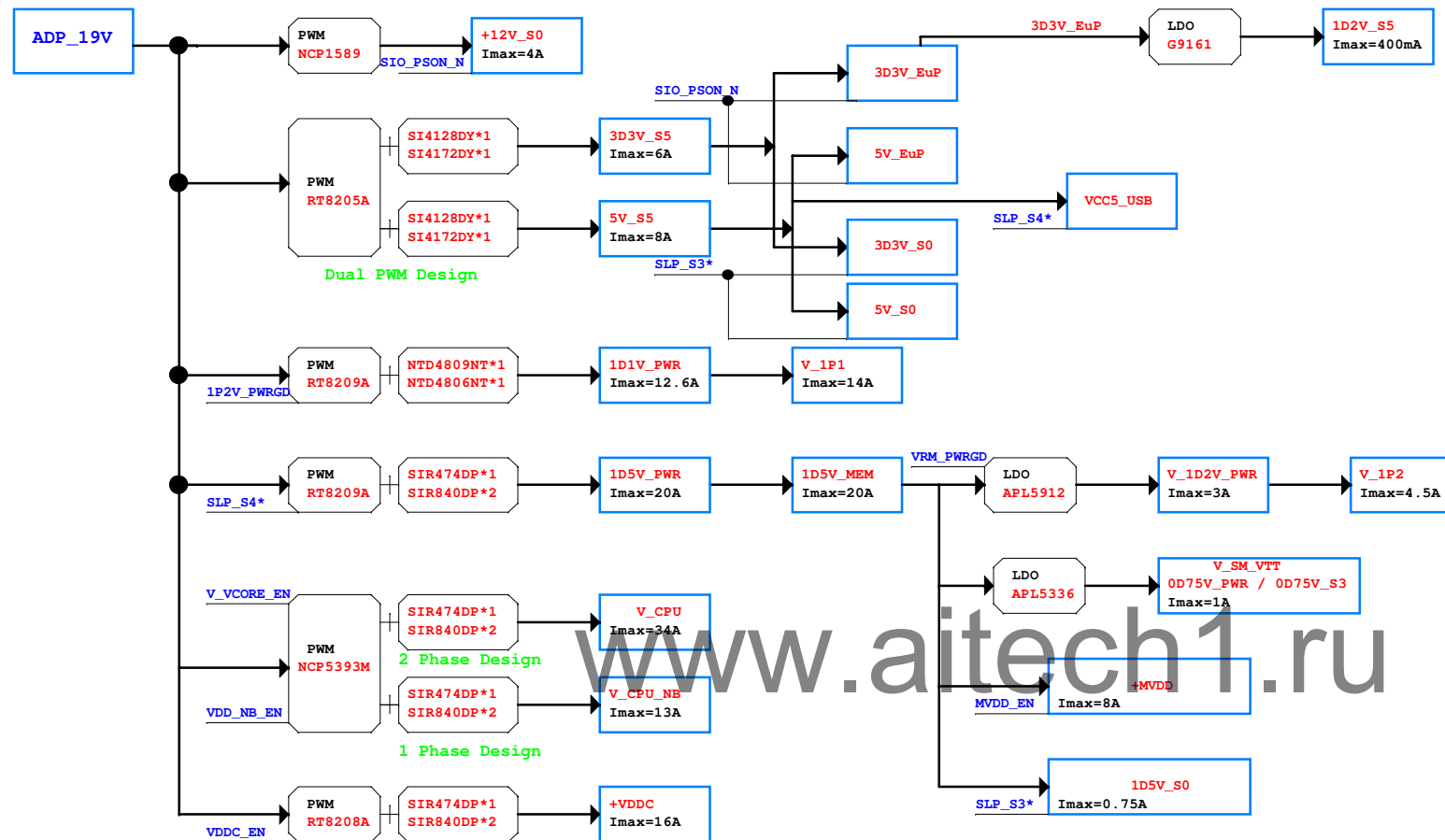
AMD RS780L+SB710  
Block Diagram

PROJECT NAME: B305  
BOARD VERSION: 1B  
DATE: 202 mm X 230 mm





DC\_IN



## CPU AM3(45W)

CPU VORE+CPU NB (0.8~1.55V 34A)
VDDR 1.2V 1.4A
CPU VDDA 2.5V 110mA
1.5V VDDIO 1.75A
VLDI 1.2V 1.4A

## RS780L

VDDHT/RX 1.1V 1.2A
VDDHTTX 1.2V 0.5A
VDDPCIE 1.1V 2A
NB CORE VDDC 1.1V 10A
VDDA18PCIE 1.8V 0.9A
PLLs 1.8V 0.1A
VDD18/VDD18_MEM 1.8V 0.01A
VDD_MEM 1.8V/1.5V 0.5A
AVDD 3.3V 0.135A

## SB710

X4 PCIE 0.8A 1.2V(S0, S1)
ATA IO 0.5A
ATA PLL 0.01A
PCIE PVDD 80mA
SB CORE 0.6A
CLOCK (S0, S1)
1.2V S5 PW 0.22A
3.3V S5 PW 0.01A
USB CORE IO 0.2A
3.3V IO 0.45A

PCIE x2 Mini Card
3D3V_S0 +3.3V 3A
+12V_S0 +12V 0.5A
1D5V_S0 +3.3VSB 0.375A

BIOS ROM(8Mb)
3D3V_S0 +3.3V 67mA

CPU Fan	System Fan
+12V_S0 +12V 0.5A	+12V_S0 +12V 0.5A

SO-DIMM
DDR3 2GB V_SM +1.5V 3A
V_SM_VTT +0.75V 1.2A

Clock Generator ICS9LPRS480AKLFT
3D3V_S0 +3.3V 0.33A

RTL8103EL
3D3V_S0 +3.3V 330mA

VT6325
3D3V_S0 +3.3V 120mA

ITE 8758E
3D3V_S0 +3.3V 120mA

USB X2 Side	USB X4 Rear	USB X4 Device
VCC5_USB 1.0A	VCC5_USB 2.0A	VCC5_USB 2.5A

3D3V_S0
LDO APL5930
1D8V (NB) Imax=1A

3D3V_S0
LDO APL5312
2D5V Imax=200mA

3D3V_S0
LDO APL5930
+1.8V_REG Imax=1.3A

3D3V_S0
LDO APL5912
+1.0V_REG Imax=1.7A

&lt;Variant Name&gt;

wistron

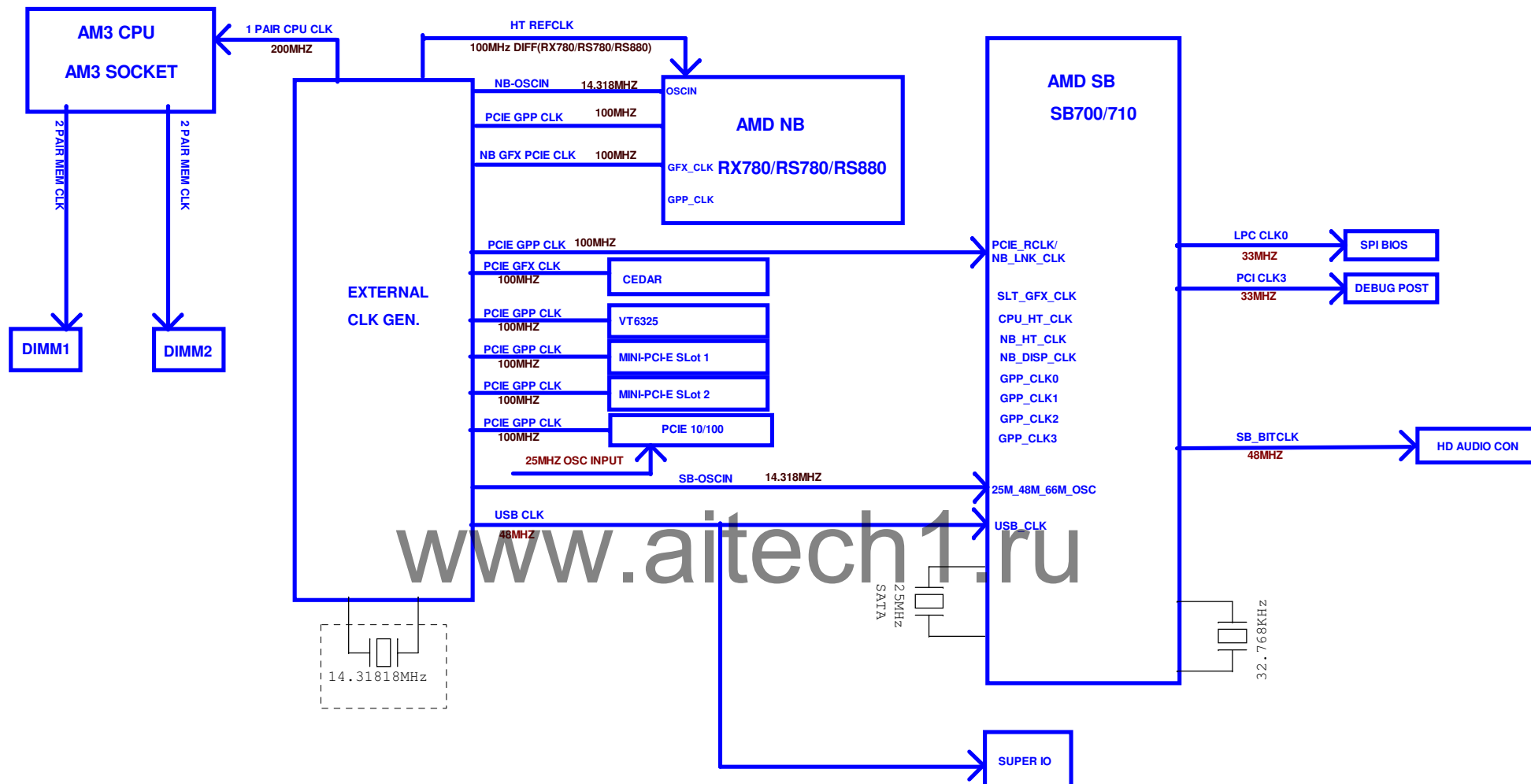
Wistron Incorporated  
21F, 88, Hein Tai Wu Rd  
Heichih, Taipei

## POWER DELIVERY CHART

Size	Document Number	Rev
C	Barbados	1B

Date: Saturday, April 28, 2010 Sheet 2 of 62





<Variant Name>

**wistron**

**Wistron Incorporated**  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

Title

**CLOCK MAP**

Size  
Custom

Document Number

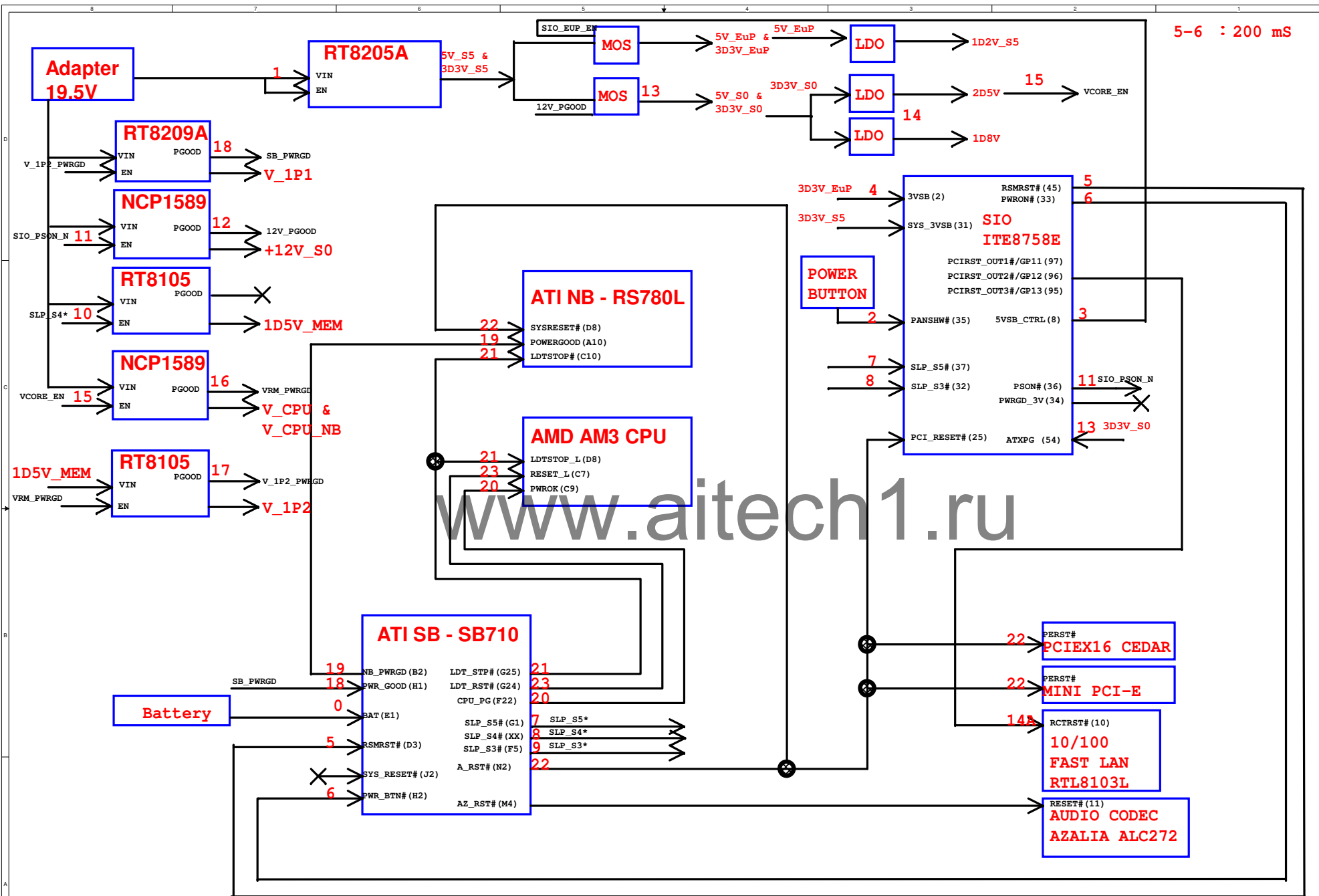
**Barbados**

Rev  
1B

Date: Saturday, April 24, 2010

Sheet 3 of 62





# RESET/POWER GOOD MAP







## GPIO Table

PIN NAME	PIN#	POWER WELL	USAGE	Default Type	Default Value	Enable Setting	Notes
GPIO0	MAIN	NO USE		GPIO	Low		Integrated Pull-down 10K
GPIO2	MAIN	SB_SPKR	Native(Speaker)	GPIO	HIGH		PC BEEP (Integrated Pull-up 8.2K)
GPIO3	MAIN	NO USE		GPIO			
GPIO4	MAIN	NO USE		GPIO			
GPIO5	MAIN	NO USE		GPIO			
GPIO6	MAIN	NO USE		GPIO			
GPIO8	MAIN	NO USE		GPIO			
GPIO9	MAIN	NO USE		GPIO			
GPIO10	MAIN	NO USE		GPIO			
GPIO11	RESUME	SPI_DATAOUT	Native(SPI ROM Data Out)	GPIO	Low		SPI Integrated Pull-down 10K
GPIO12	RESUME	SPI_DATAIN	Native(SPI ROM Data In)	GPIO	Low		SPI Integrated Pull-down 10K
GPIO13	MAIN	SPI_WMM	GPIO (Low)	GPIO	Low		SPI Write Protect
GPIO14	RESUME	NO USE		GPIO			
GPIO15	MAIN	TV_EN		GPIO	HIGH		
GPIO16	MAIN	WIRELESS_EN		GPIO	HIGH		
GPIO17	MAIN	WIRELESS_EN		GPIO	HIGH		
GPIO18	MAIN	AUTO_COLOR_SEL		GPIO	HIGH		
GPIO19	MAIN	UNUSABLE		GPIO	HIGH		
GPIO20	MAIN	NO USE		GPIO	HIGH		
GPIO21	MAIN	NO USE		GPIO	HIGH		
GPIO22	MAIN	NO USE		GPIO	HIGH		
GPIO23	MAIN	NO USE		GPIO	HIGH		
GPIO24	MAIN	NO USE		GPIO	HIGH		
GPIO25	MAIN	NO USE		GPIO	HIGH		
GPIO26	MAIN	NO USE		GPIO	HIGH		
GPIO27	MAIN	NO USE		GPIO	HIGH		
GPIO28	MAIN	NO USE		GPIO	HIGH		
GPIO29	MAIN	NO USE		GPIO	HIGH		
GPIO30	MAIN	NO USE		GPIO	HIGH		
GPIO31	RESUME	SPI_CS0	Native(SPI ROM Chip Select 0)	GPIO			Integrated Pull-up 10K
GPIO32	RESUME	SPI_CS1	Native(SPI ROM Chip Select 1)	GPIO			Integrated Pull-up 10K
GPIO33	MAIN	WIRELESS_EN		GPIO			Integrated Pull-up 8.2K
GPIO34	MAIN	NO USE		GPIO			Integrated Pull-up 8.2K
GPIO35	MAIN	NO USE		GPIO			Integrated Pull-up 8.2K
GPIO36	MAIN	NO USE		GPIO			Integrated Pull-up 8.2K
GPIO37	MAIN	NO USE		GPIO			Integrated Pull-up 8.2K
GPIO38	MAIN	NO USE		GPIO			Integrated Pull-down 10K
GPIO39	MAIN	NO USE		GPIO			Integrated Pull-down 8.2K
GPIO40	MAIN	NO USE		GPIO			Integrated Pull-down 8.2K
GPIO41	MAIN	NO USE		GPIO			Integrated Pull-down 8.2K
GPIO42	RESUME	NO USE		GPIO			Integrated Pull-down 50K
GPIO43	RESUME	AC2_DOWN	Native(HD Audio Serial Data In 1)	GPIO			Integrated Pull-down 50K
GPIO44	RESUME	NO USE		GPIO			Integrated Pull-down 50K
GPIO45	RESUME	NO USE		GPIO			Integrated Pull-down 50K
GPIO46	RESUME	NO USE		GPIO			Integrated Pull-down 50K
GPIO47	RESUME	SPI_CLK	Native(SPI ROM Clock)	GPIO			Integrated Pull-down 10K
GPIO48	MAIN	NO USE		GPIO			Integrated Pull-up 8.2K
GPIO49	MAIN	NO USE		GPIO			Integrated Pull-up 8.2K
GPIO50	MAIN	BOARD_ID	HIGH: MXM / Low: UMA	GPIO			
GPIO51	MAIN	NO USE		GPIO			
GPIO52	MAIN	NO USE		GPIO			
GPIO53	RESUME	NO USE		GPIO			
GPIO54	RESUME	NO USE		GPIO			
GPIO55	RESUME	NO USE		GPIO			
GPIO56	RESUME	NO USE		GPIO			
GPIO57	RESUME	NO USE		GPIO			
GPIO58	RESUME	NO USE		GPIO			
GPIO59	RESUME	NO USE		GPIO			
GPIO60	RESUME	NO USE		GPIO			
GPIO61	RESUME	NO USE		GPIO			
GPIO62	RESUME	NO USE		GPIO			
GPIO63	RESUME	NO USE		GPIO			
GPIO64	RESUME	TEMP_ALERT	Native(Temperature Alert)	GPIO			
GPIO65	MAIN	SD_DETECT	Native(Bus Master Request)	GPIO			
GPIO66	RESUME	NO USE		GPIO			Integrated Pull-up 10K
GPIO67	MAIN	ICH_SATA_LED	Native(Serial ATA Activity)	GPIO			OD
GPIO68	MAIN	LDOWM_SB	Native(LPC DMA Req 1)	GPIO			Integrated Pull-up 15K
GPIO69	MAIN	FP_DETECT		GPIO			Integrated Pull-up 15K
GPIO70	MAIN	NO USE		GPIO			Integrated Pull-up 15K
GPIO71	MAIN	NO USE		GPIO			
GPIO72	MAIN	NO USE		GPIO			
GPIO73	MAIN	NO USE		GPIO			

Board ID	GPIO50
MXM	1
UMA	0

## SB700 GPIO

PIN NAME	PIN#	POWER WELL	USAGE	Type	Default Type	Enable Setting	NOTES
USB_OC0#/GPM0#		RESUME	OC'01	GPIO	VCC3_3SB	LOW	
USB_OC1#/GPM1#		RESUME	OC'01	GPIO	VCC3_3SB	LOW	
USB_OC2#/GPM2#		RESUME	OC'23	GPIO	VCC3_3SB	LOW	
USB_OC3#/GPM3#		RESUME	OC'23	GPIO	VCC3_3SB	LOW	
USB_OC4#/GPM4#		RESUME	OC'45	GPIO	VCC3_3SB	LOW	
USB_OC5#/DDR3_RST#/GPM5#		RESUME	OC'45	GPIO	VCC3_3SB	LOW	
USB_OC6#/GEVENT6#		RESUME	OC'6	GPIO	VCC3_3SB	LOW	
USB_OC7#/GEVENT7#		RESUME	NO USE	GPIO	VCC3_3SB	LOW	
USB_OC8#/A2_DOCK_RST#/GPM8#		RESUME	NO USE	GPIO	VCC3_3SB	High	
USB_OC9#/SLP_S2#/GPM9#		RESUME	NO USE	GPIO	VCC3_3SB		
EXTEVENT0#		RESUME	A20GATE		VCC3_3SB		
EXTEVENT1#		MAIN	KBRST		VCC3_3SB		
GEVENT2#		RESUME	CPU_THERMTRIP		VCC3_3SB		
GEVENT3#		RESUME	LPC_PME		VCC3_3SB		
GEVENT4#		RESUME	NO USE		VCC3_3SB		
GEVENT5#		RESUME	S3_STATE		VCC3_3SB		
BLINK/GPM6#		RESUME	NO USE	GPIO	VCC3_3SB	LOW	GPM
GPM7#		RESUME	FP_RESET		VCC3_3SB		
GEVENT8#		RESUME	WOL		VCC3_3SB		
SDA0/GPOC0#		MAIN	SMBCLK		VCC3_3SB		
SDA0/GPOC1#		MAIN	SMBDATA		VCC3_3SB		
SDA1/GPOC2#		RESUME	ALERT_CLK		VCC3_3SB		
SDA1/GPOC3#			ALERT_DATA		VCC3_3SB		
IMS_GPIO13	E20		CPU_SIC				
IMS_GPIO14	E21		CPU_SID				
IMS_GPIO16	D19		IMC_GPIO16				
IMS_GPIO17	E18		IMC_GPIO17				

SOURCE	SIGNAL NAME	LINKED DEVICES
NB	DACSCL0/DACSDA0	
	DACSCL1/DACSDA1	
SB	SCLK0/SDATA0	
	SCLK1/SDATA1	

SUPER I/O: ITE 8758E



# CPU FAN

41 CPU\_FAN\_CTRL CPU\_FAN\_CTRL  
41 CPU\_FAN\_TACH CPU\_FAN\_TACH

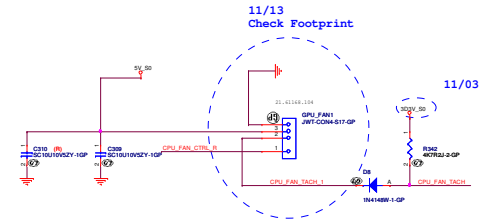
# SYSTEM FAN

41 REAR\_FAN\_CTRL REAR\_FAN\_CTRL  
41 REAR\_FAN\_TACH REAR\_FAN\_TACH

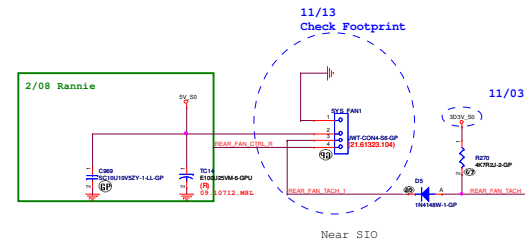
## ONLY FOR 4 PIN FAN CONTROL



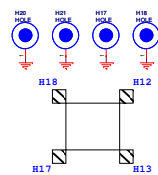
11/06



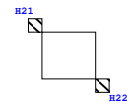
## 2nd FAN



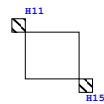
## CPU MOUNTING HOLE-PTH



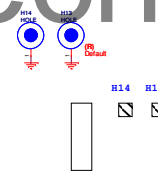
## GPU MOUNTING HOLE-NPTH



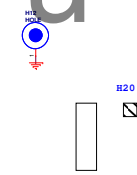
## SB MOUNTING HOLE-PTH



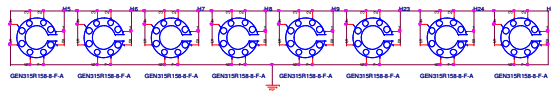
## MINI PCIE 1 MOUNTING HOLE-PTH



## MINI PCIE 1 MOUNTING HOLE-PTH



## PCB MOUNTING HOLES-PTH





# CPU CLK

10 CPUCLK CPUCLK#

# PCIEx16 CLK

54 PCIe\_REFCLK# PCIe\_REFCLKN

# LAN CLK

39 KG\_GFX\_CLKP KG\_GFX\_CLKN

# NB HCLK

17 KG\_NBHT\_CLKP KG\_NBHT\_CLKN

# NB Ref CLK

17 KG\_NBREF\_CLKP KG\_NBREF\_CLKN

# NB GFX CLK

17 KG\_NBGFY\_CLKP KG\_NBGFY\_CLKN

To SB

# Mini PCI-E CLK

1103 Modify

35 CLK\_PCE\_MINI# CLK\_PCE\_MINI#  
30 CLK\_PCE\_MINI# CLK\_PCE\_MINI#  
30 CLK\_PCE\_MINI# CLK\_PCE\_MINI#  
30 CLK\_PCE\_MINI# CLK\_PCE\_MINI#  
35 CLK\_PCE\_OR\_P CLK\_PCE\_OR\_P  
35 CLK\_PCE\_OR\_N CLK\_PCE\_OR\_N  
30 MINI\_CLKREQ# MINI\_CLKREQ#  
30 MINI\_CLKREQ# MINI\_CLKREQ#  
21,24,28,30,41,55 SMBCLK SMBCLK#  
21,24,28,30,41,55 SMBDATA SMBDATA#

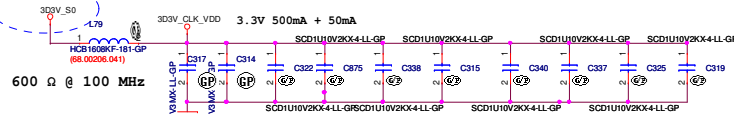
41 SIO\_CLK48 KG\_CLK\_48M\_USB

OSC\_14M\_NB

23 CLK14\_SB CLK14\_SB

47,49 1P2V\_PWRGD 1P2V\_PWRGD

11/04



11/04

11/11

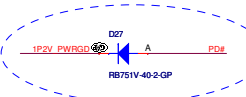
May use one 22uF instead?

## NB CLOCK INPUT TABLE

NB CLOCKS	RS780
HT_REFCLKP	100M DIFF
HT_REFCLKN	100M DIFF
REFCLK_P	1.4M SE (1.1V)
REFCLK_N	val
GFX_REFCLKP	100M DIFF
GPP_REFCLK	100M DIFF(OUT)
GPSS_REFCLK	100M DIFF

\* the GFX\_REFCLK input is required for all cases

11/03 Modify

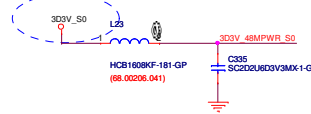


11/09

SEL_SATA_REF1	1	100 Mhz non-spreading differential SRC clock
SEL_SATA_REF0	0	100 Mhz spreading differential SRC clock
SEL_HIT66_REF0	1	86 Mhz 3.3V single ended HTT clock
	0	100 Mhz differential HTT clock

\* default

11/04



Due to PLL issue on current clock chip, the SBlk clock need to come from SRC clocks for RS740 and RS780. Future clock chip revision will fix this.

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

www.aitech.com

11/06 Ryan suggest

KG\_NBREF\_CLKP R787 1  
KG\_NBREF\_CLKN R788 1  
CLK\_PCE\_MINI# R789 1  
CLK\_PCE\_MINI# R790 1  
CLK\_PCE\_MINI# R791 1  
CLK\_PCE\_MINI# R792 1  
CLK\_PCE\_OR\_P R793 1  
CLK\_PCE\_OR\_N R794 1  
MINI\_CLKREQ# R795 1  
MINI\_CLKREQ# R796 1  
KG\_GFX\_CLKP R797 1  
KG\_GFX\_CLKN R798 1

KG\_SBLINK\_CLKP R801 1  
KG\_SBLINK\_CLKN R802 1

KG\_NBHT\_CLKP R803 1  
KG\_NBHT\_CLKN R804 1

HTT07\_LPRS66M HTT07\_LPRS66M  
HTT08\_LPRS66M HTT08\_LPRS66M

KG\_NBHT\_CLKP R805 1  
KG\_NBHT\_CLKN R806 1

KG\_NBHT\_CLKP R807 1  
KG\_NBHT\_CLKN R808 1

KG\_NBHT\_CLKP R809 1  
KG\_NBHT\_CLKN R810 1

KG\_NBHT\_CLKP R811 1  
KG\_NBHT\_CLKN R812 1

KG\_NBHT\_CLKP R813 1  
KG\_NBHT\_CLKN R814 1

KG\_NBHT\_CLKP R815 1  
KG\_NBHT\_CLKN R816 1

KG\_NBHT\_CLKP R817 1  
KG\_NBHT\_CLKN R818 1

KG\_NBHT\_CLKP R819 1  
KG\_NBHT\_CLKN R820 1

KG\_NBHT\_CLKP R821 1  
KG\_NBHT\_CLKN R822 1

11/11

11/06 Ryan suggest

KG\_NBREF\_CLKP R787 1  
KG\_NBREF\_CLKN R788 1  
CLK\_PCE\_MINI# R789 1  
CLK\_PCE\_MINI# R790 1  
CLK\_PCE\_MINI# R791 1  
CLK\_PCE\_MINI# R792 1  
CLK\_PCE\_OR\_P R793 1  
CLK\_PCE\_OR\_N R794 1  
MINI\_CLKREQ# R795 1  
MINI\_CLKREQ# R796 1  
KG\_GFX\_CLKP R797 1  
KG\_GFX\_CLKN R798 1

KG\_SBLINK\_CLKP R801 1  
KG\_SBLINK\_CLKN R802 1

KG\_NBHT\_CLKP R803 1  
KG\_NBHT\_CLKN R804 1

HTT07\_LPRS66M HTT07\_LPRS66M  
HTT08\_LPRS66M HTT08\_LPRS66M

KG\_NBHT\_CLKP R805 1  
KG\_NBHT\_CLKN R806 1

KG\_NBHT\_CLKP R807 1  
KG\_NBHT\_CLKN R808 1

KG\_NBHT\_CLKP R809 1  
KG\_NBHT\_CLKN R810 1

KG\_NBHT\_CLKP R811 1  
KG\_NBHT\_CLKN R812 1

KG\_NBHT\_CLKP R813 1  
KG\_NBHT\_CLKN R814 1

KG\_NBHT\_CLKP R815 1  
KG\_NBHT\_CLKN R816 1

KG\_NBHT\_CLKP R817 1  
KG\_NBHT\_CLKN R818 1

KG\_NBHT\_CLKP R819 1  
KG\_NBHT\_CLKN R820 1

KG\_NBHT\_CLKP R821 1  
KG\_NBHT\_CLKN R822 1

For NB GFX

For PCIEx16

11/03 CLKREQ# Internal pull high

11/14

11/04

11/04

11/04

11/04

11/04

11/04

11/04

11/04

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11/04

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<Variant Name>

wistron

Wistron Incorporated  
21F, 88, Hei Tai Wu Rd  
Hsichih, Taipei

EXTERNAL CLOCK GENERATOR

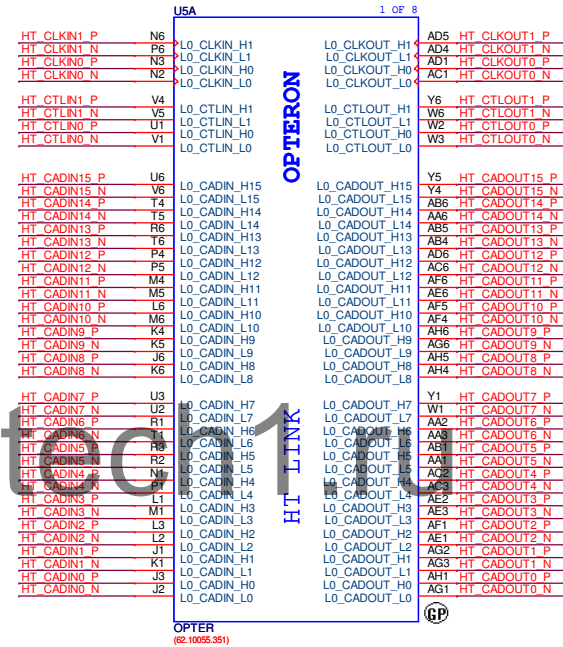
Barbados

Date: Saturday, April 24, 2010 Sheet 8 of 62



# HT Interface

15 HT_CLKIN1_P	>> HT_CLKIN1_P
15 HT_CLKIN1_N	>> HT_CLKIN1_N
15 HT_CLKIN0_P	>> HT_CLKIN0_P
15 HT_CLKIN0_N	>> HT_CLKIN0_N
15 HT_CTLIN1_P	>> HT_CTLIN1_P
15 HT_CTLIN1_N	>> HT_CTLIN1_N
15 HT_CTLIN0_P	>> HT_CTLIN0_P
15 HT_CTLIN0_N	>> HT_CTLIN0_N
15 HT_CLKOUT1_P	<< HT_CLKOUT1_P
15 HT_CLKOUT1_N	<< HT_CLKOUT1_N
15 HT_CLKOUT0_P	<< HT_CLKOUT0_P
15 HT_CLKOUT0_N	<< HT_CLKOUT0_N
15 HT_CTLOUT1_P	<< HT_CTLOUT1_P
15 HT_CTLOUT1_N	<< HT_CTLOUT1_N
15 HT_CTLOUT0_P	<< HT_CTLOUT0_P
15 HT_CTLOUT0_N	<< HT_CTLOUT0_N
15 HT_CADIN7_P	>> HT_CADIN7_P
15 HT_CADIN7_N	>> HT_CADIN7_N
15 HT_CADIN6_P	>> HT_CADIN6_P
15 HT_CADIN6_N	>> HT_CADIN6_N
15 HT_CADIN5_P	>> HT_CADIN5_P
15 HT_CADIN5_N	>> HT_CADIN5_N
15 HT_CADIN4_P	>> HT_CADIN4_P
15 HT_CADIN4_N	>> HT_CADIN4_N
15 HT_CADIN3_P	>> HT_CADIN3_P
15 HT_CADIN3_N	>> HT_CADIN3_N
15 HT_CADIN2_P	>> HT_CADIN2_P
15 HT_CADIN2_N	>> HT_CADIN2_N
15 HT_CADIN1_P	>> HT_CADIN1_P
15 HT_CADIN1_N	>> HT_CADIN1_N
15 HT_CADIN0_P	>> HT_CADIN0_P
15 HT_CADIN0_N	>> HT_CADIN0_N
15 HT_CADIN15_P	>> HT_CADIN15_P
15 HT_CADIN15_N	>> HT_CADIN15_N
15 HT_CADIN14_P	>> HT_CADIN14_P
15 HT_CADIN14_N	>> HT_CADIN14_N
15 HT_CADIN13_P	>> HT_CADIN13_P
15 HT_CADIN13_N	>> HT_CADIN13_N
15 HT_CADIN12_P	>> HT_CADIN12_P
15 HT_CADIN12_N	>> HT_CADIN12_N
15 HT_CADIN11_P	>> HT_CADIN11_P
15 HT_CADIN11_N	>> HT_CADIN11_N
15 HT_CADIN10_P	>> HT_CADIN10_P
15 HT_CADIN10_N	>> HT_CADIN10_N
15 HT_CADIN9_P	>> HT_CADIN9_P
15 HT_CADIN9_N	>> HT_CADIN9_N
15 HT_CADIN8_P	>> HT_CADIN8_P
15 HT_CADIN8_N	>> HT_CADIN8_N
15 HT_CADOUT7_P	<< HT_CADOUT7_P
15 HT_CADOUT7_N	<< HT_CADOUT7_N
15 HT_CADOUT6_P	<< HT_CADOUT6_P
15 HT_CADOUT6_N	<< HT_CADOUT6_N
15 HT_CADOUT5_P	<< HT_CADOUT5_P
15 HT_CADOUT5_N	<< HT_CADOUT5_N
15 HT_CADOUT4_P	<< HT_CADOUT4_P
15 HT_CADOUT4_N	<< HT_CADOUT4_N
15 HT_CADOUT3_P	<< HT_CADOUT3_P
15 HT_CADOUT3_N	<< HT_CADOUT3_N
15 HT_CADOUT2_P	<< HT_CADOUT2_P
15 HT_CADOUT2_N	<< HT_CADOUT2_N
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15 HT_CADOUT13_P	<< HT_CADOUT13_P
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15 HT_CADOUT10_P	<< HT_CADOUT10_P
15 HT_CADOUT10_N	<< HT_CADOUT10_N
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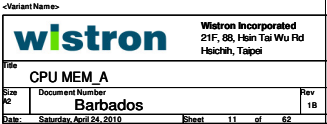
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Title <b>CPU HT Interface</b>			
Size A3	Document Number <b>Barbados</b>		Rev 1B
Date: Saturday, April 24, 2010	Sheet 9	of 62	



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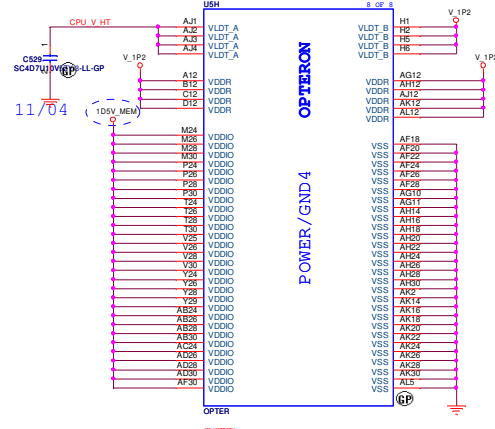
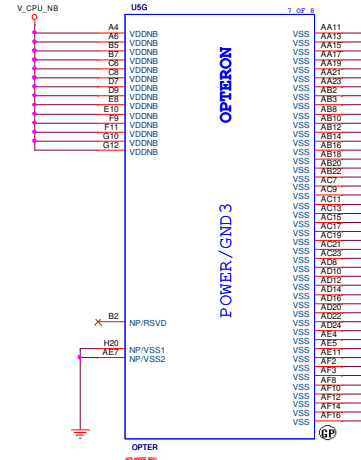
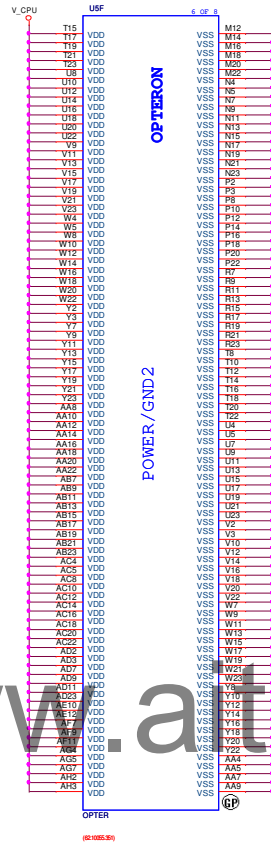
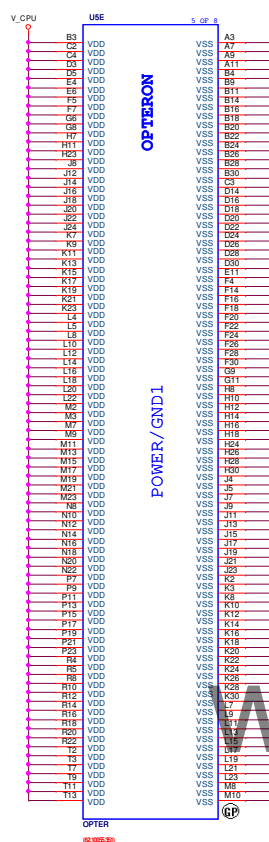
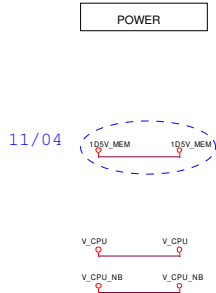






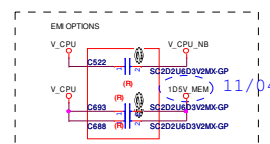
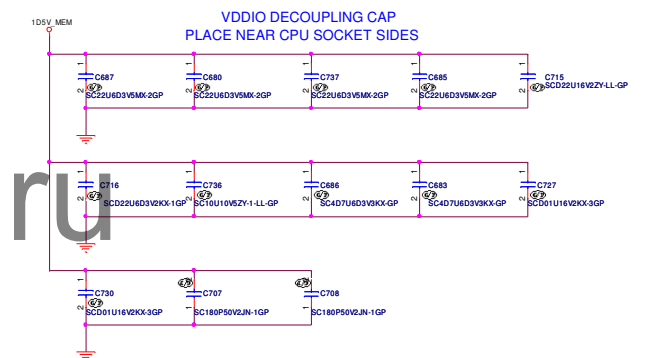
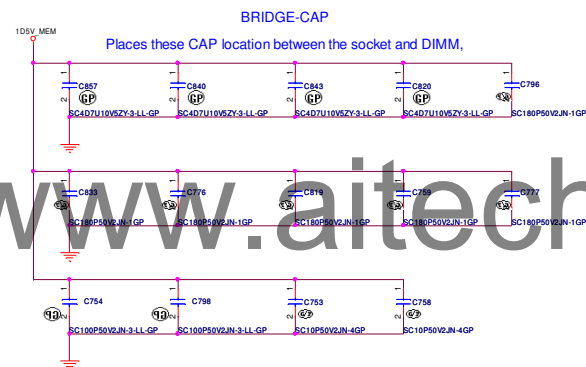
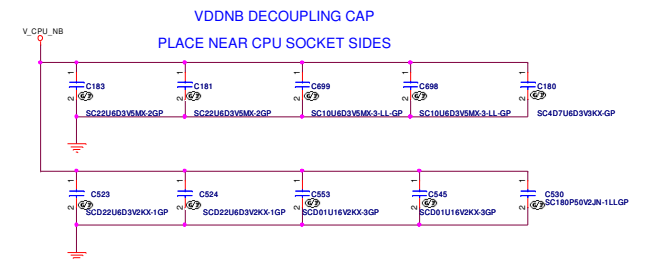
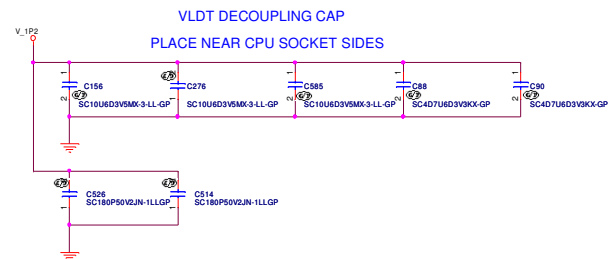






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SC22U6D3V5MX-2GP -- CHIP CAP C 22U 6.3V M0805 X5R
SC10U6D3V5MX-3-LL-GP -- CHIP CAP C 10U 6.3V M0805 X5R
SC4D7U10V5ZY-3-LL-GP -- CHIP CAP C 4.7U 10V Z0805 Y5V
SCD22U16V2ZY-1GP -- CHIP CAP C 0.22U 16V Z0402 Y5V
SCD01U16V2KX-3GP -- CHIP CAP0.01U16V K0402 X7R(ROH)
SC180P50V2JN-1GP -- CHIP CAPACITOR C 180P 50V J0402 NPO
SC100P50V2JN-3-LL-GP -- CHIP CAPACITOR C 100P 50V J0402 NPO
```

CHIP CAP C 4.7U 6.3V 0603 X5R 78.47520.5BL  
CHIP CAP C .22U 6.3V 0402 X5R 78.22420.5FL



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9 HT\_CADOUT0\_N >>> HT\_RXCAD0\_N  
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9 HT\_CADOUT1\_N >>> HT\_RXCAD1\_N  
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9 HT\_CADOUT8\_P >>> HT\_RXCAD8\_P  
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HT\_TXCTL1\_N >>> HT\_CTLIN1\_N

USA		1 OF 6	
HT_RXCAD0_P	Y25	HT_TXCAD0P	D24
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HT_RXCAD1_P	Y22	HT_TXCAD1P	E24
HT_RXCAD1_N	Y23	HT_TXCAD1N	E25
HT_RXCAD2_P	V25	HT_TXCAD2P	F24
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HT_RXCAD3_P	U24	HT_TXCAD3P	F23
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HT_RXCAD8_P	AC24	HT_TXCAD8P	F21
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HT_RXCAD14_P	U21	HT_TXCAD14P	M21
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HT_RXCAD15_P	U19	HT_TXCAD15P	P18
HT_RXCAD15_N	U18	HT_TXCAD15N	M18
HT_RXCLK0_P	T22	HT_TXCLK0P	H24
HT_RXCLK0_N	T23	HT_TXCLK0N	H25
HT_RXCLK1_P	AB23	HT_TXCLK1P	L21
HT_RXCLK1_N	AA22	HT_TXCLK1N	L20
HT_RXCTL0_P	M22	HT_TXCTL0P	M24
HT_RXCTL0_N	M23	HT_TXCTL0N	M25
HT_RXCTL1_P	P21	HT_TXCTL1P	P19
HT_RXCTL1_N	P20	HT_TXCTL1N	R18
HT_RXCALP	C23	HT_TXCALP	B24
HT_RXCALN	A24	HT_TXCALN	B25

Place < 100 mils  
from C23 and A24

(71.RS780.M15)

Place < 100 mils  
from B24 and B25

RS780/RS740/RS780 difference table (HT LINK)

SIGNALS	RS740	RS780	RS780
HT_RXCALP	49.9R (GND)	121K	301R
HT_RXCALN	49.9R (VDDHT)		
HT_TXCALP	100R	121K	301R
HT_TXCALN			

<Variant Name>

**wlstron**

Wistron Incorporated  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

Title  
RS780L-HT LINK0 V/F

Size  
Custom

Document Number  
Barbados

Rev  
1B

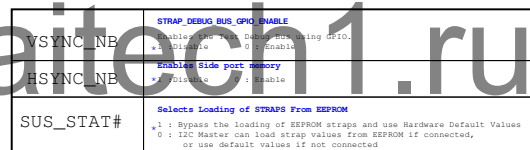
Date: Saturday, April 24, 2010

Sheet 15 of 62
















5					4					3					2					1				
D																								
C																								
B																								
A																								

RESERVED


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<Variant Name>									
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Title RS760 (RESERVED)									
Size A		Document Number Barbados						Rev 1B	
Date: Saturday, April 24, 2010					Sheet 19 of 62				



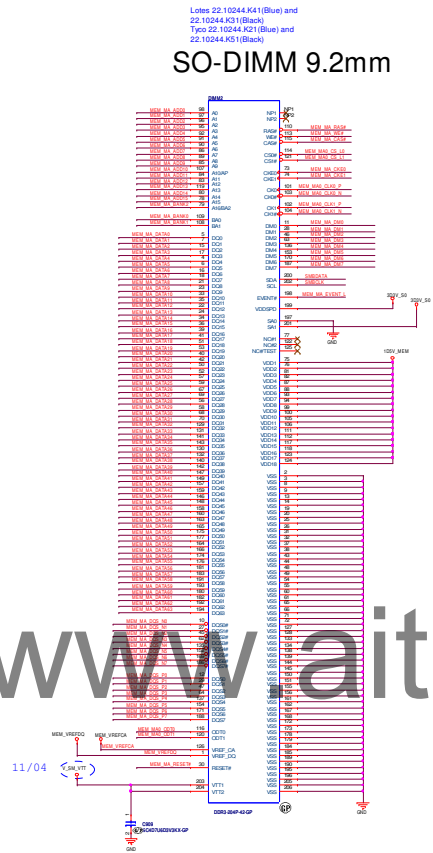
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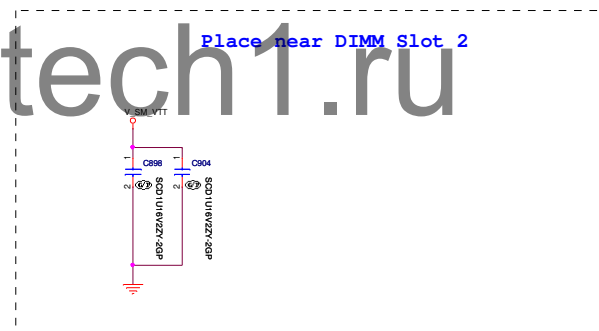
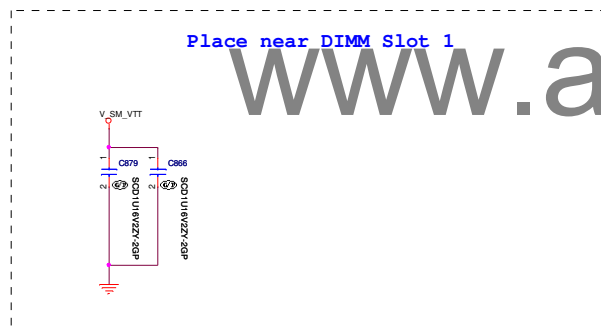
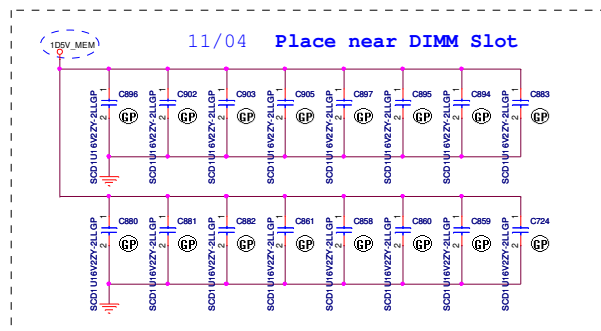
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Size A	Document Number Barbados	Rev 1B
Date: Saturday, April 24, 2010	Sheet 20	of 62



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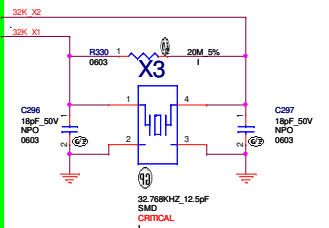
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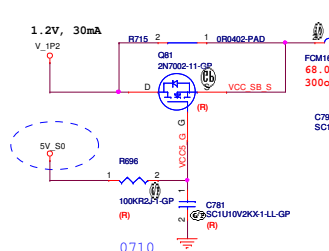




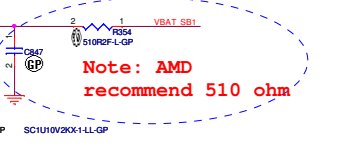
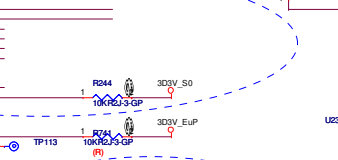
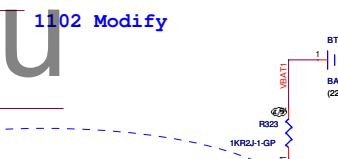
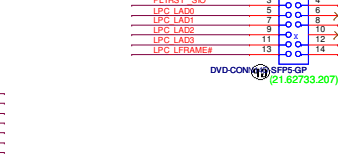
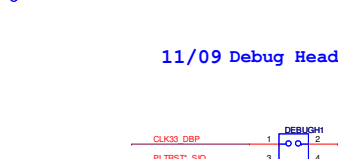
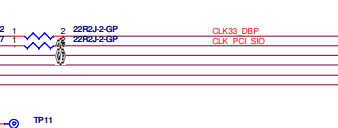
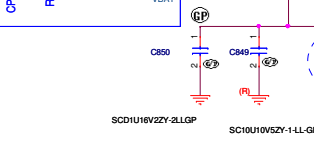
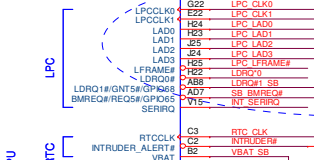
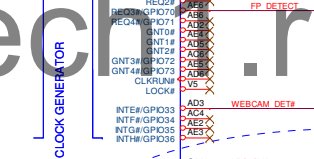
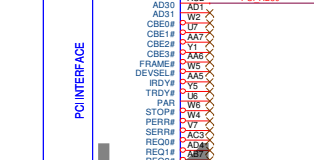
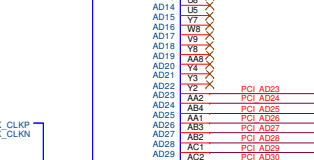
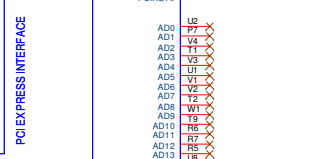
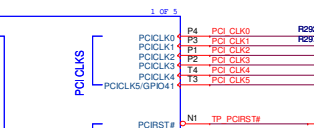
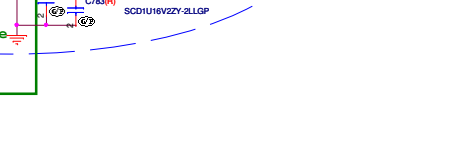
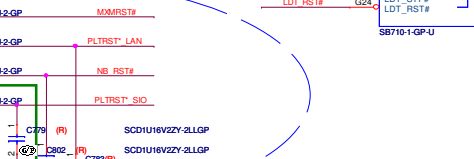
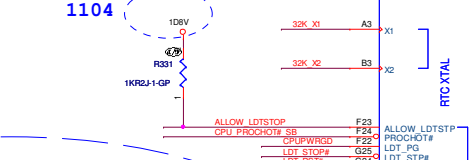
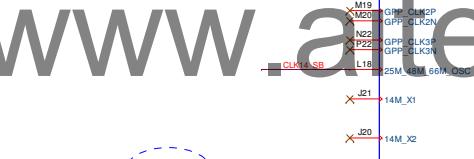
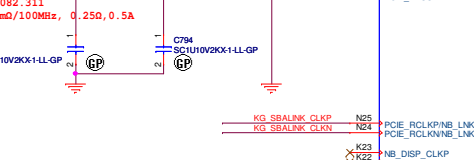
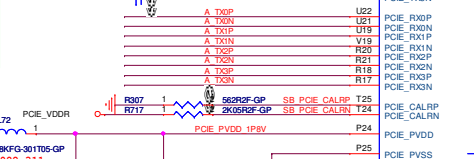
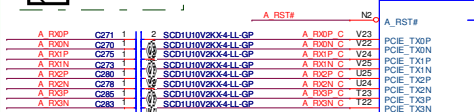
Close to SB710 12/30



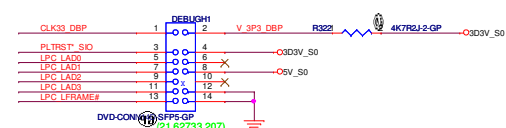
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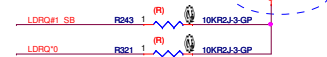
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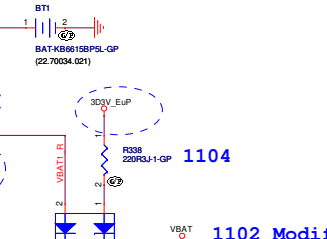
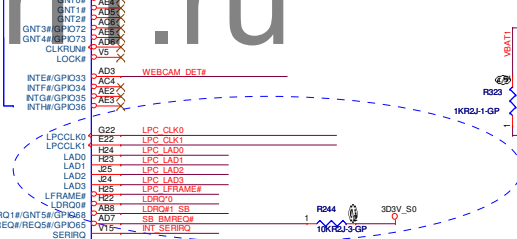
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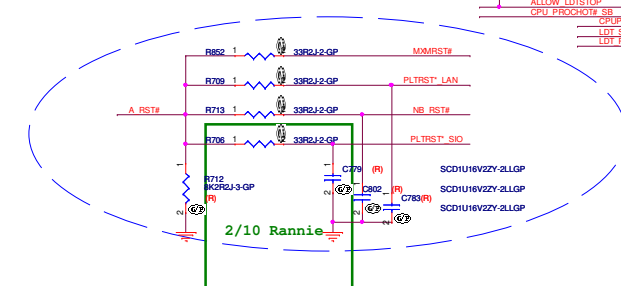
11/04



1102 Modify

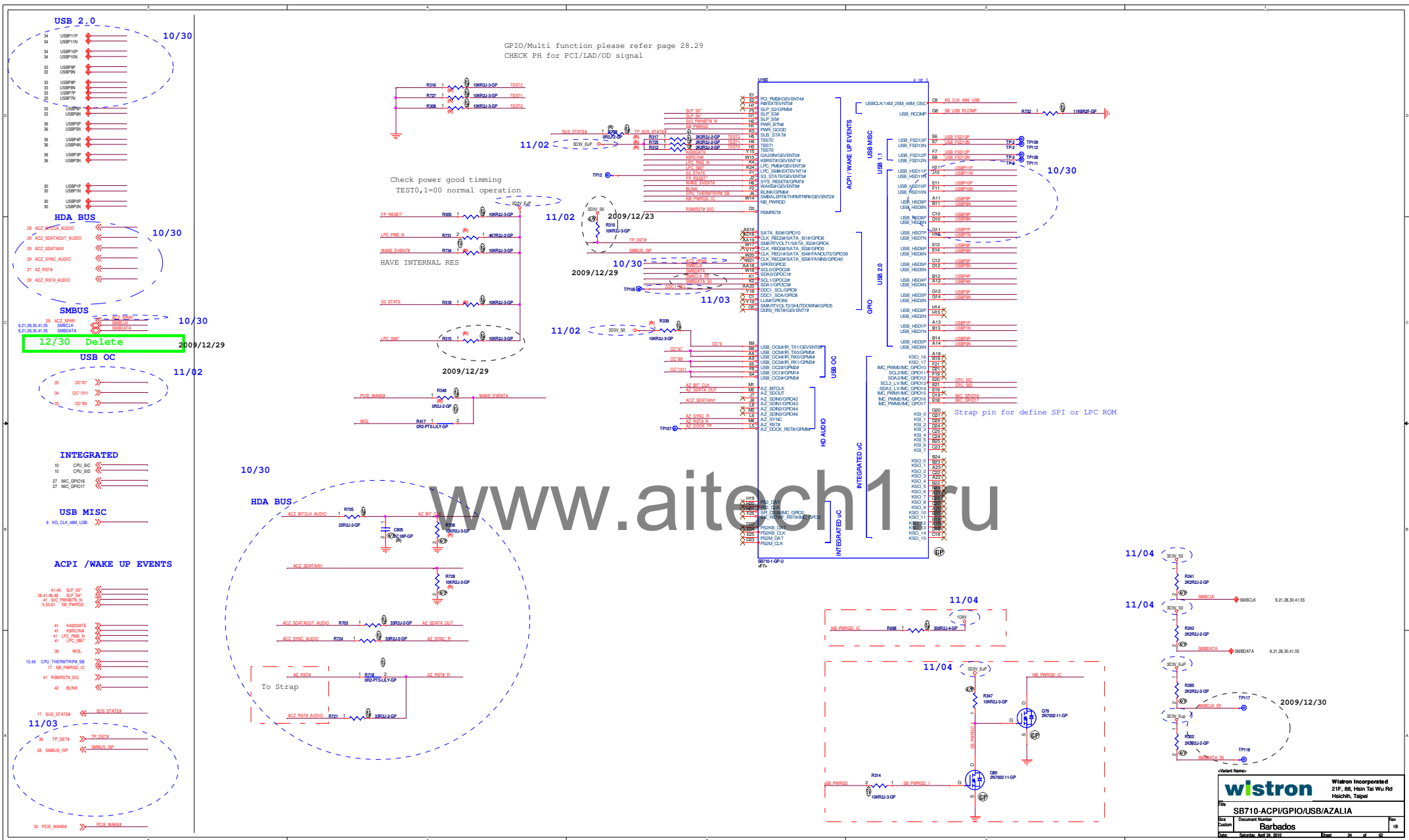


Note: AMD recommend 510 ohm



2/10 Ranni







Interface	Signal Name	Pull-up/down	Resistor Value (Ω)
IDE	PIDE_DRQ	Pull-down	50k
	PIDE_DRQ	Pull-up	5.6k ± 20%
	PIDE_CORDY	Pull-up	4.7k ± 20%
	SIDE_CORDY	Pull-up	4.7k ± 20%
	PIDE_IRQ	Pull-down	10k ± 20%
	SIDE_IRQ	Pull-down	10k ± 20%
	PIDE_D7	Pull-down	10k ± 20%
USB	SIDE_D0	Pull-down	10k ± 20%
	48M_X1USBCLK	Pull-down	50k
AC '97	USB_HSDAT[7:0]	Pull-down	15k ± 20%
	USB_HSDAT[7:0]	Pull-up	15k ± 20%
	AC_BTCLK	Pull-down	50k
Processor	AC_SDINCE[5]	Pull-down	50k
	A20M#	Pull-up	1.25k ± 20%
	CFU_PG	Pull-up	1.25k ± 20%
	FERR#	Pull-up	1.25k ± 20%
	IGNEN#	Pull-up	1.25k ± 20%
	INT#	Pull-up	1.25k ± 20%
	INTRLINT	Pull-up	1.25k ± 20%
	MMIO_LINT1	Pull-up	1.25k ± 20%
	SM#	Pull-up	1.25k ± 20%
	STPCLK#/ALLOW_LDSTP#	Pull-up	1.25k ± 20%

11/10

11/03

10 T\_ALERT\$ >> T\_ALERT\$

11/03

11/07

2009/12/23

```

34 LAN_100LED_CTRL    << LAN_100LED_CTRL
34 LAN_LINKED_CTRL    << LAN_LINKED_CTRL
42 WLAN_LED#_CTRL     << WLAN_LED#_CTRL
42 LVDS_LED_CTRL       << LVDS_LED_CTRL
42 BT_LED_PWR_CTRL     << BT_LED_PWR_CTRL
55 GPU_WP#             << GPU_WP#

```

3/12 Rannie modify

**NOTE :**  
R528 IS 1K 1% FOR 25MHz  
XTAL, 4.99K 1% FOR 100MHz  
INTERNAL CLOCK

**NOTE :**  
DSG-215SB600-10.pdf, page 17  
When NOT using the serial ATA interface:  
a. Leave the SATA transmit and receive pairs unconnected  
b. Leave the SATA\_ACT#, SATA\_CAL, and SATA\_X2 balls unconnected.  
c. Connect SATA\_X1 ball to GND.

1118 Modify

68.00082.311  
300ohmΩ/100MHz, 0.25Ω, 0.5A

11/03

1102 Modify

2/08 Rannie

1. Main Source: 72.25X80.A01 (Winbond 8Mb)
2. 2nd Source: 72.25805.001 (MXIC 8Mb)
3. 3ns source: 72.26081.001 (ATMEL 8Mb)

<Variant Name>



**Wistron Incorporated**  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

Title  
SB710-SATA/IDE

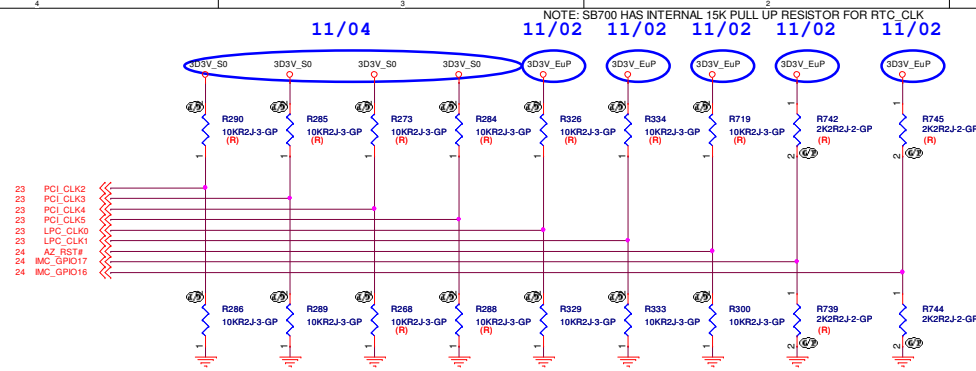
Size	Document Number
Custom	Barbados

Date: Saturday, April 24, 2010 Sheet 25 of 62









## REQUIRED STRAPS

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	AZ_RST#	IMC_GPIO17	IMC_GPIO16
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	IMC ENABLED	ROM TYPE: H, H = Reserved NC, L = SPI ROM DEFAULT	
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	IMC DISABLED DEFAULT	L, H = LPC ROM L, L = FWH ROM	

2009/12/23

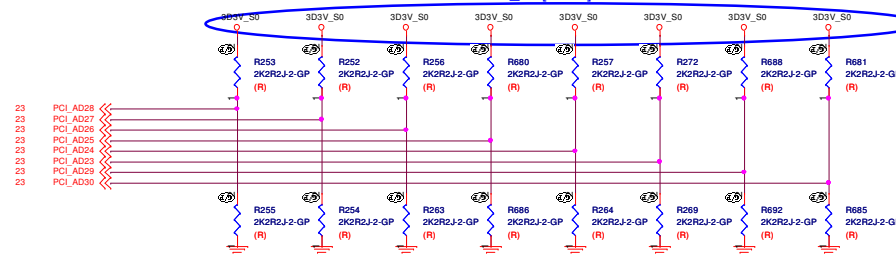


OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

## DEBUG STRAPS

11/04

SB700 HAS 15K INTERNAL PU FOR PCI\_AD[30:23]



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD29 PCI_AD30
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOTFAILTIMER DISABLED DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED	

<Variant Name>

<b>wistron</b>		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
File SB710 STRAPS			
Size Custom	Document Number Barbados	Rev 1B	
Date: Saturday, April 24, 2010		Sheet 27 of 62	







```

24 ACZ_RST#_AUDIO >>> ACZ_RST#_AUDIO
24 ACZ_SYNC_AUDIO >>> ACZ_SYNC_AUDIO
24 ACZ_SDATANI >>> ACZ_SDATANI
24 ACZ_BITCLK_AUDIO >>> ACZ_BITCLK_AUDIO
24 ACZ_SDATAOUT_AUDIO >>> ACZ_SDATAOUT_AUDIO
24 ACZ_SPKR >>> ACZ_SPKR

```

**IN** 40 MIC\_R\_JACK >>> MIC\_R\_JACK  
40 MIC\_L\_JACK >>> MIC\_L\_JACK

40 ALC272\_HP\_OUT\_R <<<\_\_\_\_\_

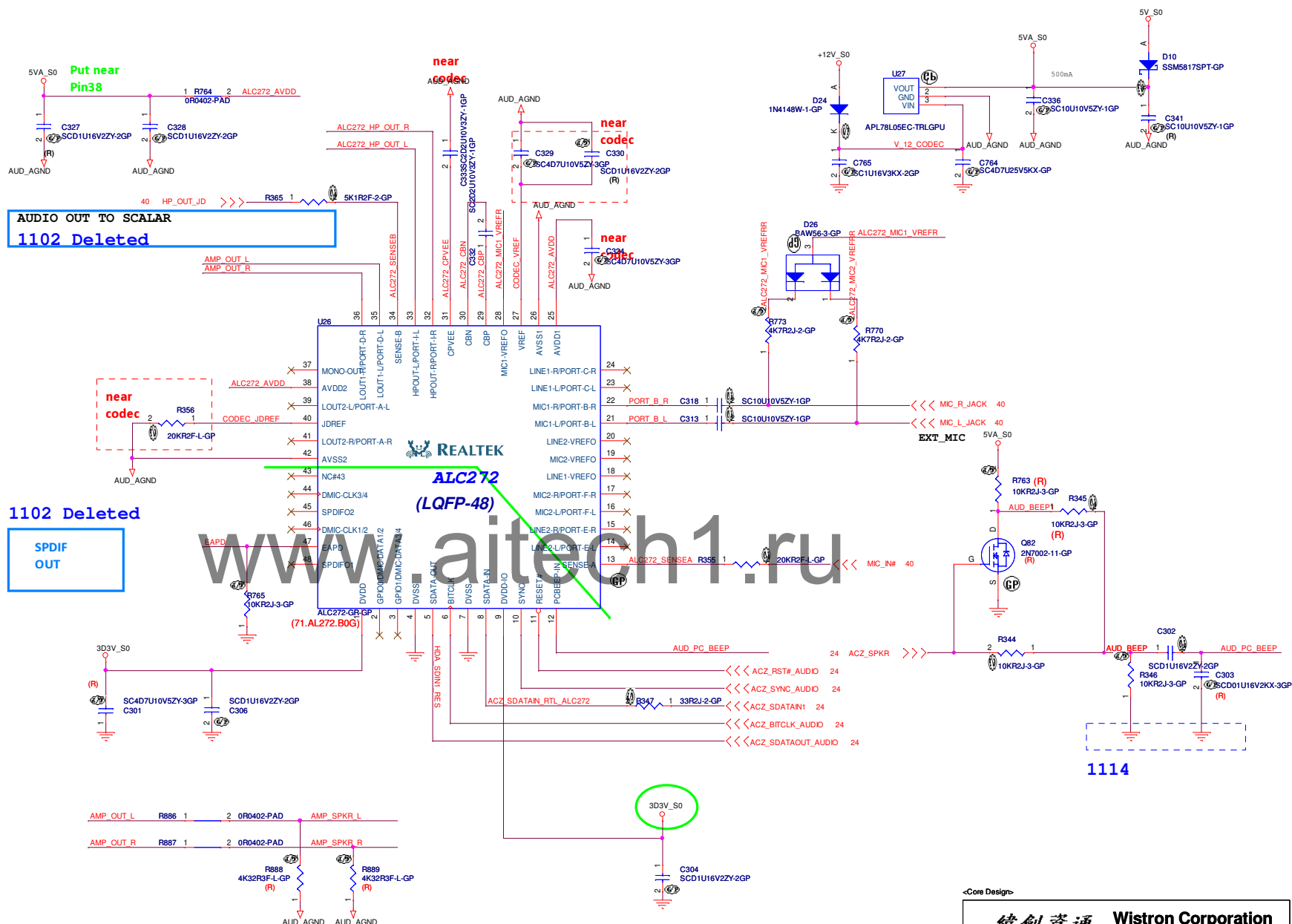
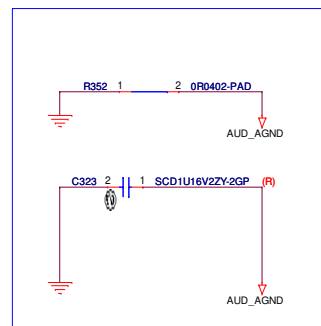
40 ALC272\_HP\_OUT\_L <<<\_\_\_\_\_

**Detect**

38 EAPD <<< EAPD

38 AMP\_SPKR\_L <<< AMP\_SPKR\_L

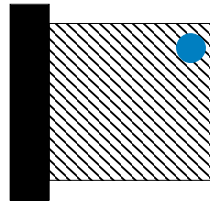
38 AMP\_SPKR\_R <<< AMP\_SPKR\_R



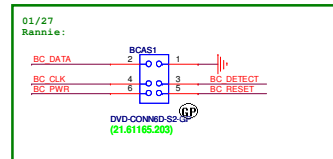
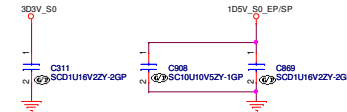
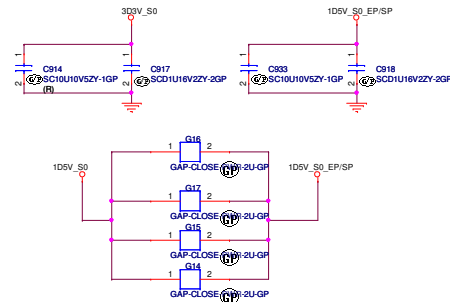
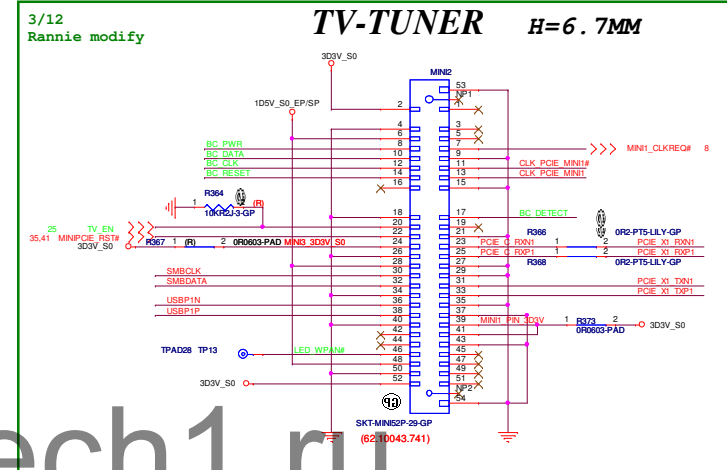
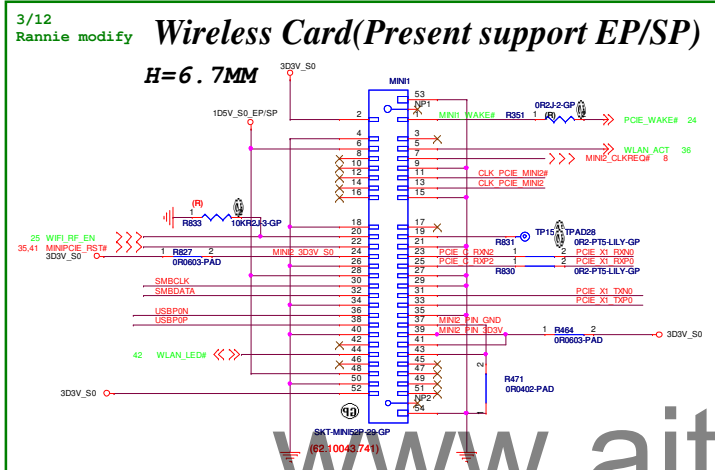
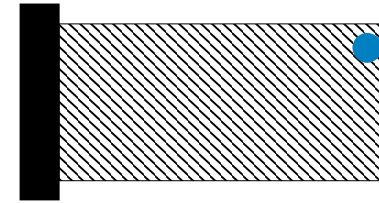


# Mini PCI-E Connector

Half Mini PCI-E CARD



Full Mini PCI-E CARD



<Variant Name>

**wlstron**

Wistron Incorporated  
21F, 88, Hei Tai Wu Rd  
Hsichih, Taipei

Title		MINI PCIE Slot	
Size	Document Number	New	
C	Barbados	18	
Date:	Saturday, April 24, 2010	Sheet	30 of 62



## RGB

17 VGA\_RED >> VGA\_RED  
17 VGA\_GREEN >> VGA\_GREEN  
17 VGA\_BLUE >> VGA\_BLUE

55 M\_RED >> M\_RED  
55 M\_GREEN >> M\_GREEN  
55 M\_BLUE >> M\_BLUE

## H/VSNC

17 VSYNC\_NB >> VSYNC\_NB  
17 HSYNC\_NB >> HSYNC\_NB  
55.58 GMCH\_VSYNC >> GMCH\_VSYNC  
55.58 GMCH\_HSYNC >> GMCH\_HSYNC

## DDC\_CLK/DATA

17 VGA\_PCH\_DDCSCL << VGA\_PCH\_DDCSCL  
17 VGA\_PCH\_DDCSDA << VGA\_PCH\_DDCSDA  
55 GMCH\_DDC\_DATA << GMCH\_DDC\_DATA  
55 GMCH\_DDC\_CLK << GMCH\_DDC\_CLK

## GPIO

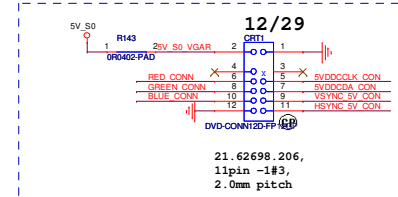
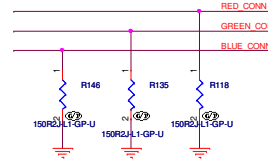
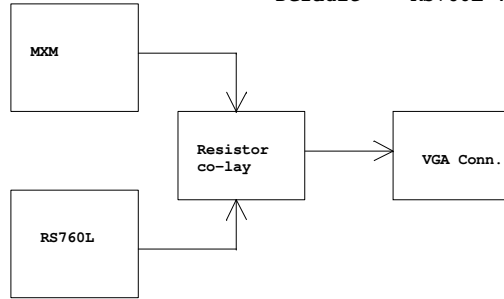
## Switch Signal to RTD2280L

28 SVDCCCLK\_CON >> SVDCCCLK\_CON  
28 SVDCCDA\_CON >> SVDCCDA\_CON  
28 VSYNC\_SV\_CON >> VSYNC\_SV\_CON  
28 HSYNC\_SV\_CON >> HSYNC\_SV\_CON  
28 RED\_CONN >> RED\_CONN  
28 GREEN\_CONN >> GREEN\_CONN  
28 BLUE\_CONN >> BLUE\_CONN

# Topology

For User Switch and Debugger

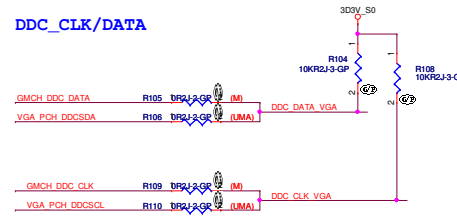
Default : RS760L VGA



## RGB



## DDC\_CLK/DATA

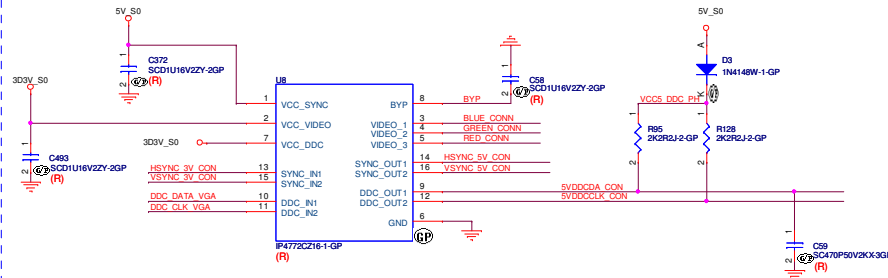


## H/VSNC



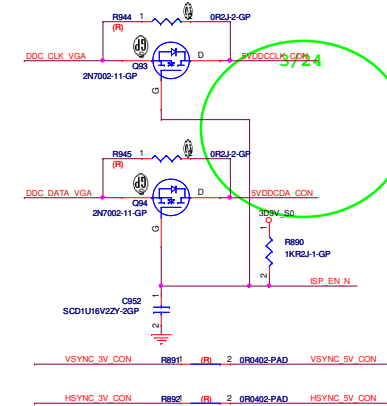
01/28

Rannie: VGA path 1



01/28

Rannie: VGA path 2



**wistron**

Wistron Incorporated  
12F, 88, Hsin Tai Wu Rd  
Hsinchu, Taipei

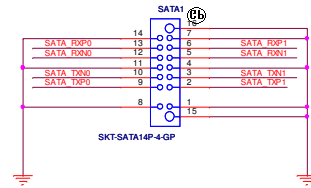
Title: VGA Switch  
Size: C  
Document Number: Barbados  
Date: Saturday, April 24, 2010  
Sheet: 31 of 62



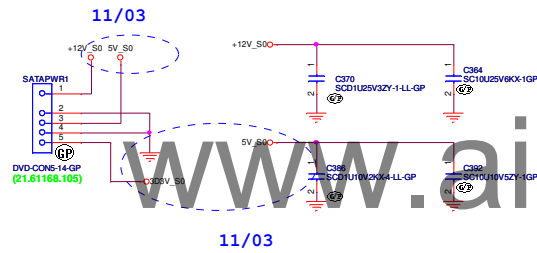
SATA\_HD

SATA\_CD\_ROM

25	SATA_RXP1_C	<<	C873	1	SC001U18V2KX3GP	SATA_RXP1
25	SATA_RXN1_C	<<	C877	1	SC001U18V2KX3GP	SATA_RXN1
25	SATA_TXP1_C	<<	C887	1	SC001U18V2KX3GP	SATA_TXP1
25	SATA_TXN1_C	<<	C884	1	SC001U18V2KX3GP	SATA_TXN1
25	SATA_RXP0_C	<<	C885	1	SC001U18V2KX3GP	SATA_RXP0
25	SATA_RXN0_C	<<	C888	1	SC001U18V2KX3GP	SATA_RXN0
25	SATA_TXP0_C	<<	C893	1	SC001U18V2KX3GP	SATA_TXP0
25	SATA_TXN0_C	<<	C891	1	SC001U18V2KX3GP	SATA_TXN0



3.5" SATA HDD power connector



Slim SATA ODD power connector

11/30

Delete ODD POWER CONN.

Because it could be combined in other conn.

www.aitech1.ru

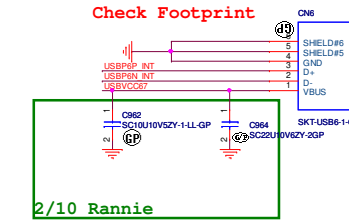
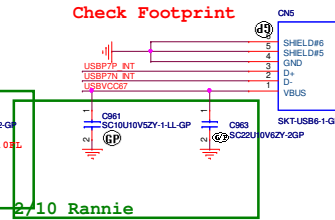
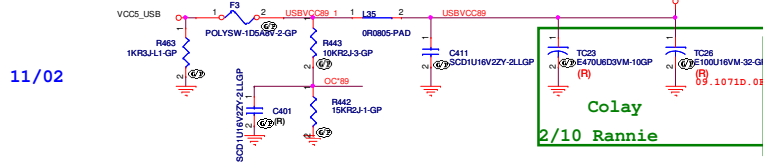
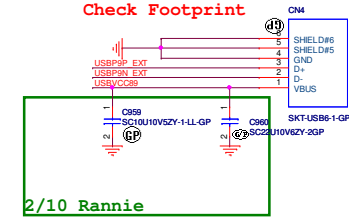
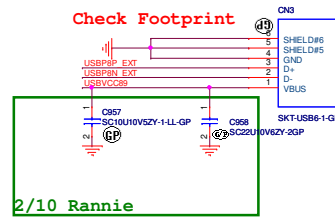
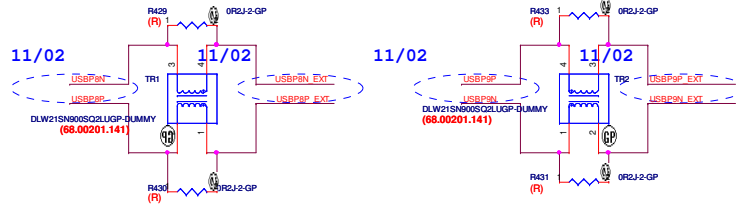
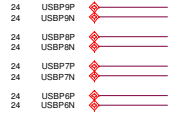
<Variant Name>

<b>wlstron</b>		<b>Wistron Incorporated</b> 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title <b>SATA CONN</b>			
Size C	Document Number <b>Barbados</b>		Rev 1B
Date:	Saturday, April 28, 2010	Sheet	32 of 62

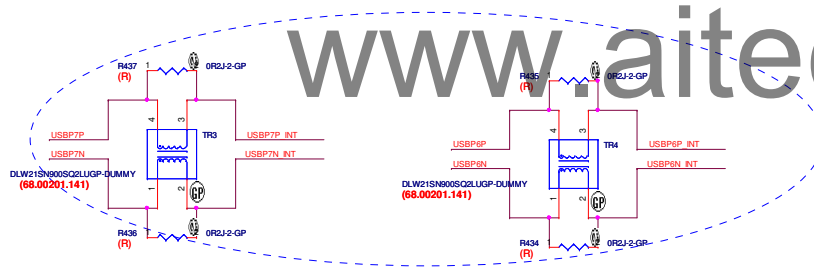
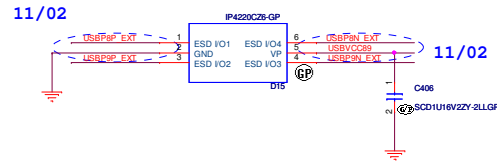


## REAR 4 USB PORT

USB PORT X4

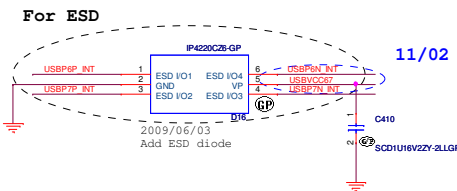
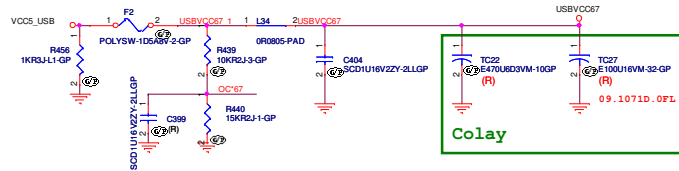


For ESD



www.aitech1.ru

11/02



<Variant Name>

**wlstron**

Wistron Incorporated  
21F, 88, Hei Tai Wu Rd  
Hsichih, Taipei

FRONT USB HEADER

Document Number  
**Barbados**

Date: Saturday, April 24, 2010 Sheet 33 of 62



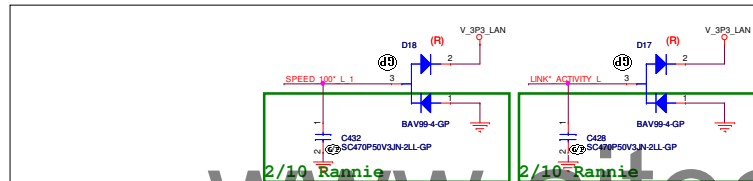
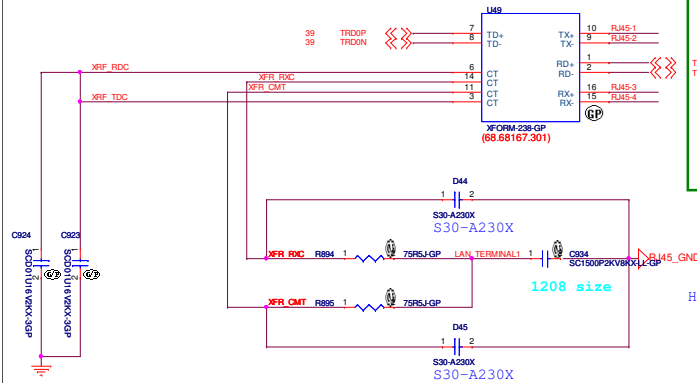
24 USBP11P  
24 USBP11N  
24 USBP10P  
24 USBP10N

24 OC\*1011  
25 LAN\_100LED\_CTRL  
25 LAN\_LINKLED\_CTRL

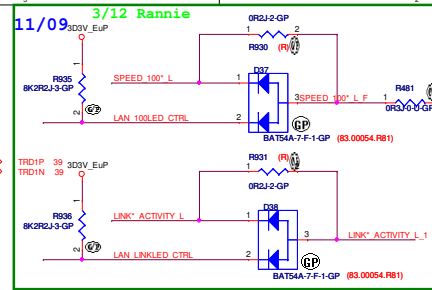
39 SPEED\_10\*\_L  
39 SPEED\_100\*\_L  
39 LINK\*\_ACTIVITY\_L  
39 TRDOP  
39 TRDON  
39 TRD1P  
39 TRD1N

01/29  
Lenovo suggestion

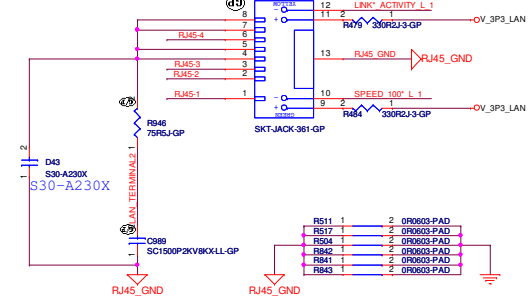
10/100M Lan Transformer



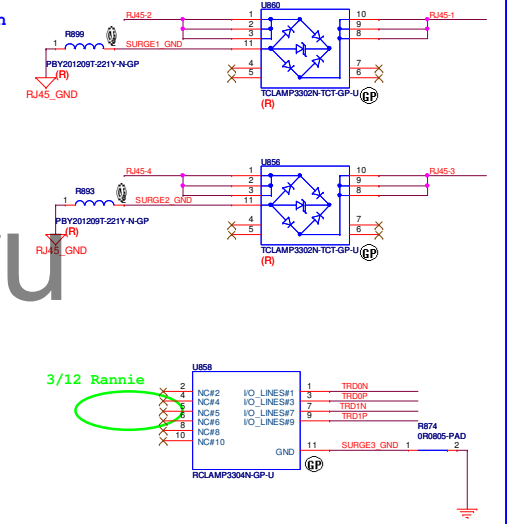
H16 connected to GND for LAN ESD protector



Check Footprint 2010/01/05

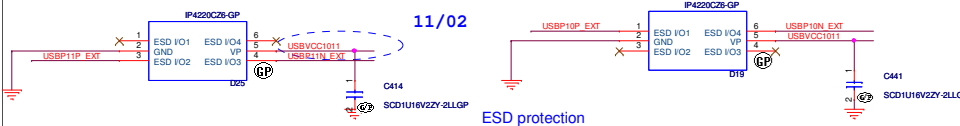


2010/01/05  
LAN Surge Solution



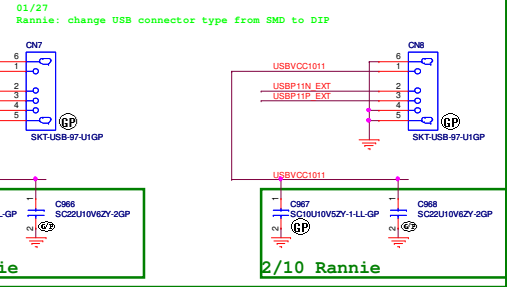
Side 2 USB PORT  
(2/3)

For ESD



Colay  
2/10 Rannie

3/12 Rannie





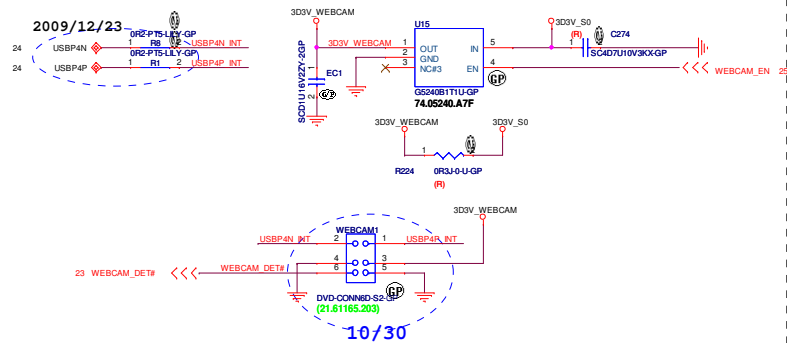




## CAMERA

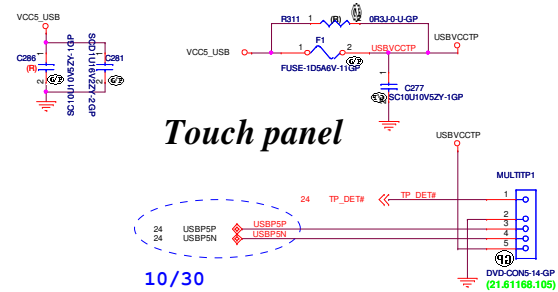
10/30

2009/12/23



WEBCAM	WEBCAM Function
L	Cable inserted
H	Cable not inserted

nextwindow 1950 series

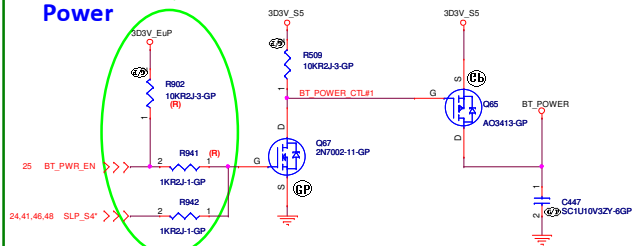


TP_DET#	Nextwindow Function
L	Cable inserted
H	Cable not inserted

0201 Rannie modify

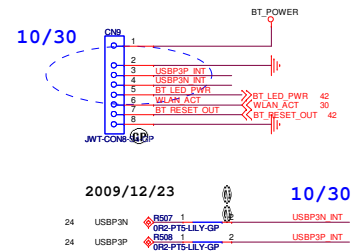
Blue  
Tooth  
Power


3/24







BT_PWR_EN GPIO51(S5 power)	Blue Tooth Power
L	Disable
H	Enable

Blue  
Tooth

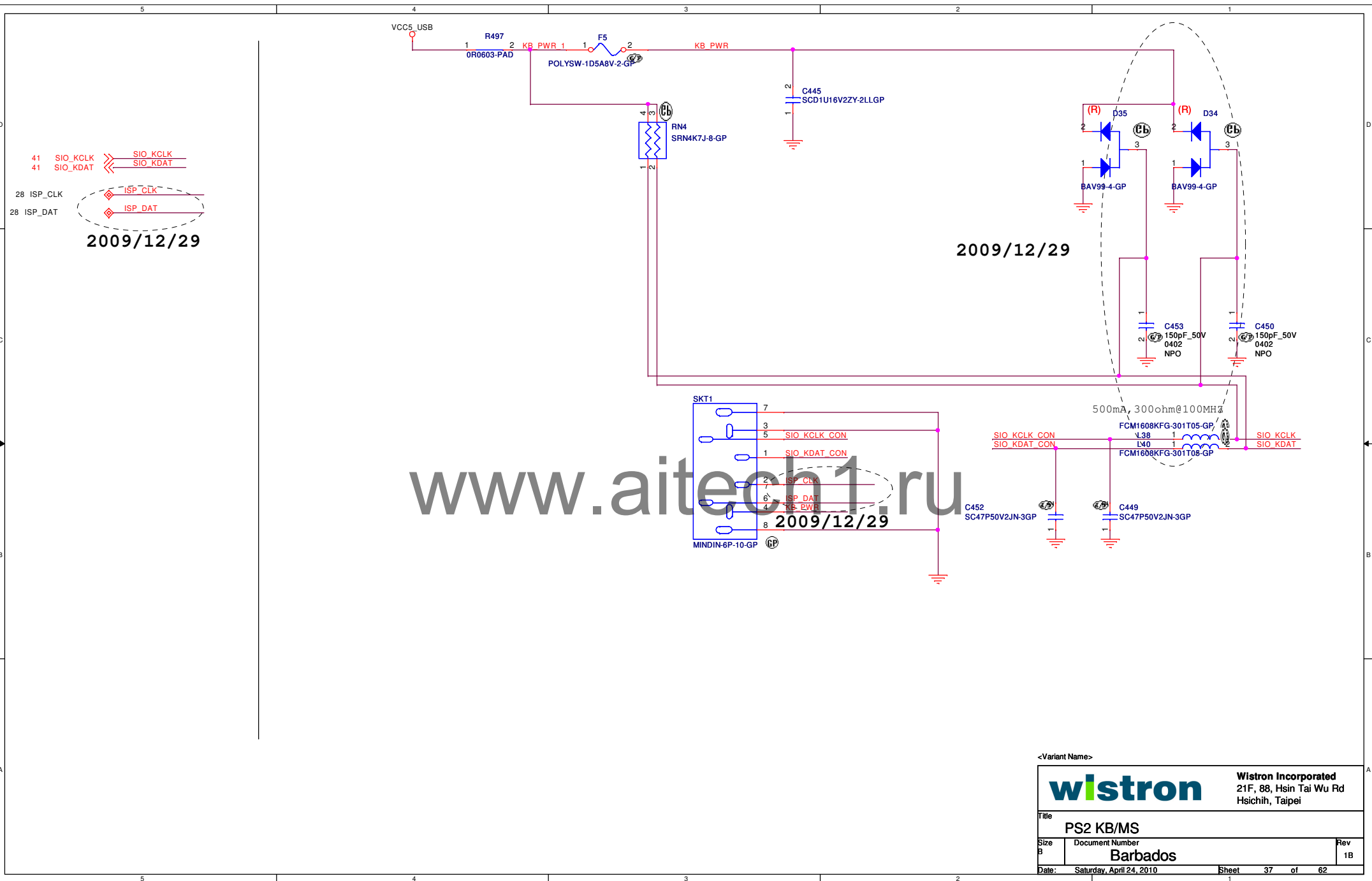


2009/12/23  10/30

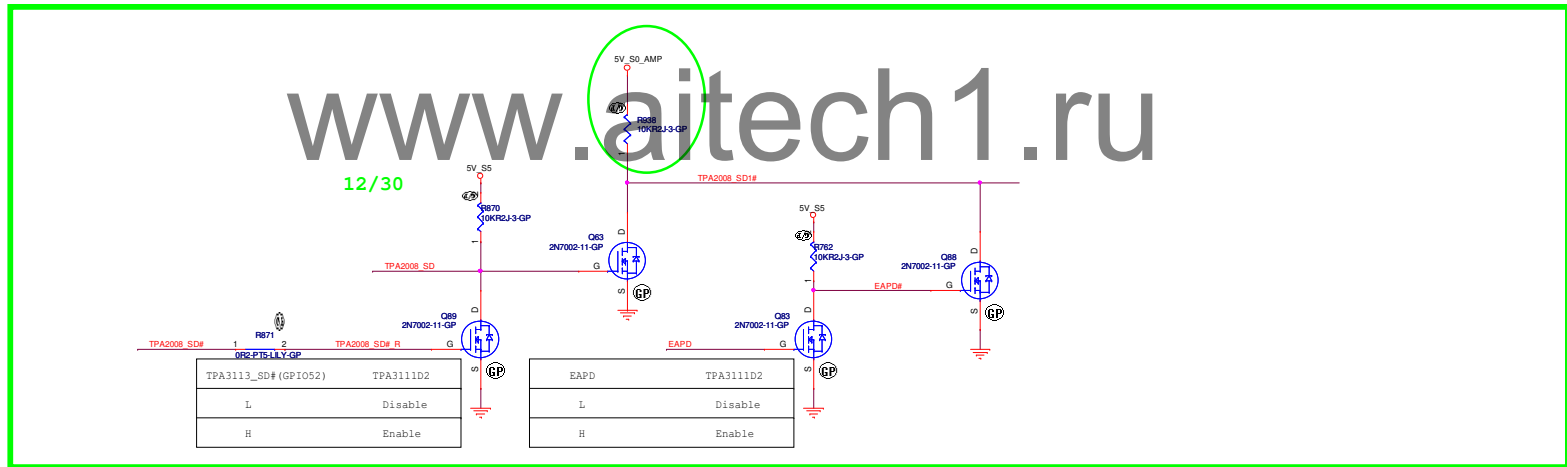
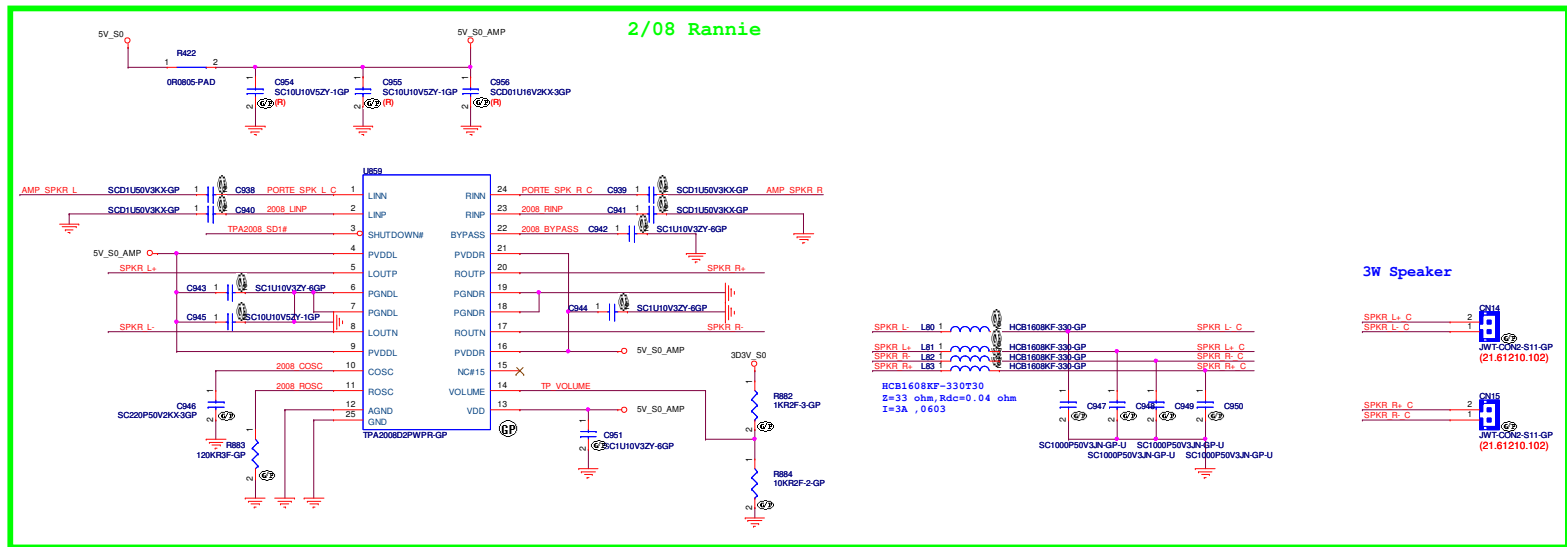
24 USBP3N  R507 1  USBP3N INT

24 USBP3P  R508 1  2 USBP3P INT











16 PCIE\_GLAN\_RXP << PCIE\_GLAN\_RXP 1 C395 PCIE\_LAN\_TXP\_ICH  
SCDU10V2KX-4-LL-GP

16 PCIE\_GLAN\_RXN << PCIE\_GLAN\_RXN 1 C384 PCIE\_LAN\_TXN\_ICH  
SCDU10V2KX-4-LL-GP

16	PCIE_GLAN_TXP	PCIE TXP LAN
16	PCIE_GLAN_TXN	PCIE TXN LAN

8 KG\_GFX\_CLKP >>> \_\_\_\_\_

8 KG\_GFX\_CLKN >>> \_\_\_\_\_

23 PLTRST\* LAN >>>

24 WOL >>

34 TRD0P

34 TRD0N

34 TRD1P

34 TRD1N

3D3V EuP

1 R483 2 0R0855-PAD

C427 C396 C412 C420

SC42U10W5Z-3L6G SC42U10W5Z-2L6G

V 3P3 LAN

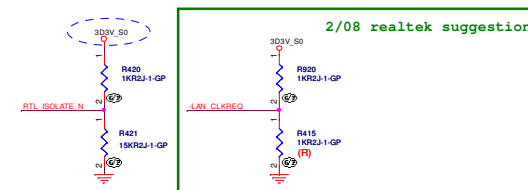
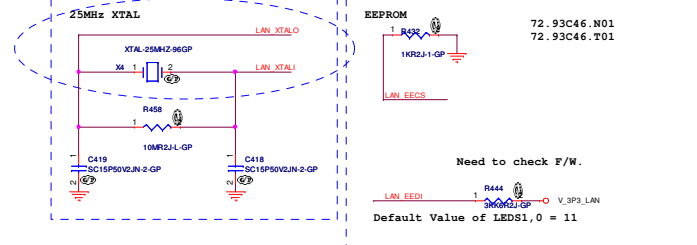
V 3P3 LAN

Close to Pin 1, 29, 37

Close to Pin 10,13,30,36

1. The trace length between R105 and 8103EL pin1 must be within 200mil.
2. C57 to R584 must be within 200mil.
3. The trace width from VDD33 to pin45 should>40mils.
4. Power plane for pin48 and around ground trace.

1. Pin48 should be near R449, and then 0.1uF(C56).
2. Pin 45 should be near 0.1u F(C57).





**Codecs** MIC\_L\_JACK  
29 MIC\_R\_JACK

HP  
From  
out  
Scalar

ALC272\_HP\_OUT\_L  
29 ALC272\_HP\_OUT\_R

ALC272\_HP\_OUT\_L  
ALC272\_HP\_OUT\_R

**JACK DETECT**

29 MIC\_IN# >>> MIC\_IN#

29 HP\_OUT\_JD >>> HP\_OUT\_JD

38 TPA2008\_SD      >> TPA2008 SD

12/30  
01/04

TPA3113_SD (GPIO52)	HEADER
L	Enable
H	Disab

HP  
OUT

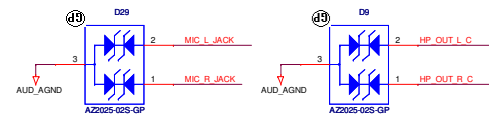
Normal: open, Jack in: short

12/30

MIC  
IN

FRONT MIC JACK (21/22)

**Check  
Footprint**



If use:  
83.02025.0A1

If use:  
83.02025.0A1



# Fan Controller

11/03

7 CPU\_FAN\_TACH  
7 CPU\_FAN\_CTRL  
7 REAR\_FAN\_TACH  
7 REAR\_FAN\_CTRL

CPU\_FAN\_TACH  
CPU\_FAN\_CTRL  
REAR\_FAN\_TACH  
REAR\_FAN\_CTRL

# LPC interface

Please check it's pull-high location

23 LPC\_LAD0  
23 LPC\_LAD1  
23 LPC\_LAD2  
23 LPC\_LAD3  
24 KBCRNM  
24 KAR0GATE  
23 CLK\_P0\_SIO  
23 PLTRST\_SIO  
23 INT\_SERRIO

LPC\_LAD0#  
LPC\_LAD1#  
LPC\_LAD2#  
LPC\_LAD3#  
KBCRNM#  
KAR0GATE#  
CLK\_P0\_SIO  
PLTRST\_SIO  
INT\_SERRIO

37 SIO\_KCLK  
37 SIO\_KDAT  
24 RSMRST#\_SIO  
44 SIO\_PSON\_N  
49 PWROD0V\_150MS  
42 SIO\_PWRLED\_N  
24 SIO\_PWNBTN\_N  
42 PWRBTN\_N  
24 LPC\_PWE\_N  
24.46 SLP\_S3\*  
24.36,46,48 SLP\_S4\*  
10 CPU\_THERM0  
10 CPU\_THERM0  
55 GPU\_DPLUS  
55 GPU\_DMINUS

SIO\_KCLK  
SIO\_KDAT  
RSMRST#\_SIO  
SIO\_PSON\_N  
PWROD0V\_150MS  
SIO\_PWRLED\_N  
SIO\_PWNBTN\_N  
PWRBTN\_N  
LPC\_PWE\_N  
SLP\_S3\*  
SLP\_S4\*  
CPU\_THERM0  
CPU\_THERM0  
GPU\_DPLUS  
GPU\_DMINUS

11/04

24 LPC\_SMI#  
4 SIO\_CLK#

LPC\_SMI#  
SIO\_CLK#

11/07  
12/30

3/16 Rannie modify

2/04 Rannie modify

2/04 Rannie modify

2/04 Rannie modify

2/04 Rannie modify

2/04 Rannie modify

2/04 Rannie modify

2/04 Rannie modify

2/04 Rannie modify

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2009/12/23

# SuperIO Power-Save

Install N-Mos and Current-Limit Resistor when in S5 for power-saving.

303V\_S0

303V\_EUP

303V\_S0

303V\_EUP

303V\_S0

303V\_EUP

303V\_S0

303V\_EUP

303V\_S0

303V\_EUP

303V\_S0

303V\_EUP

303V\_S0

303V\_EUP

303V\_S0

303V\_EUP

303V\_S0

303V\_EUP

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303V\_EUP

303V\_S0

303V\_EUP

303V\_S0

303V\_EUP

303V\_S0

303V\_EUP

303V\_S0

303V\_EUP

303V\_S0

303V\_EUP

303V\_S0

303V\_EUP

303V\_S0

303V\_EUP

# SuperIO power monitoring inputs

Please set R value depend on what you need.

11/04

11/06

11/04

2/10 Rannie

11/04

11/06

11/04

2/10 Rannie

11/04

11/06

11/04

2/10 Rannie

11/04

11/06

11/04

2/10 Rannie

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2/10 Rannie

11/04

11/06

11/04

2/10 Rannie

11/04

11/06

11/04

2/10 Rannie

If without use these pins, Please pull-up. Don't let it floating

1.Pin 54:VIN3/ATXPG

2.Pin 32:SUSB#

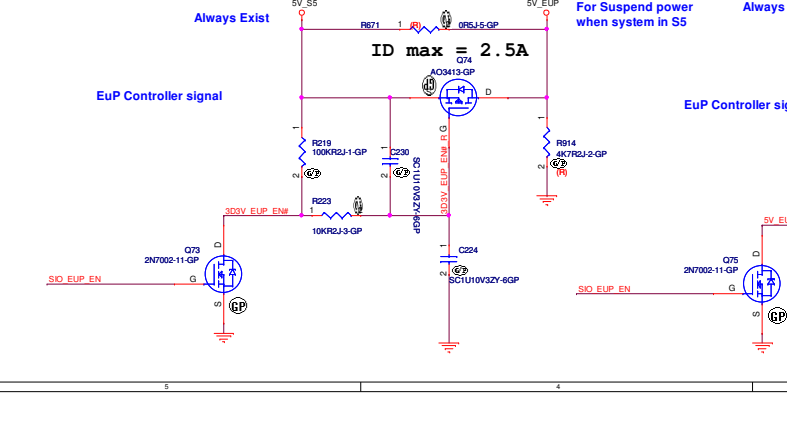
3.Pin 23/ Pin 58/ Pin 60/ Pin 62

4.Pin55 need 2.8V

Note:use EUP function:Pin32/Pin33/Pin34/Pin37/Pin39/Pin45 pull high to SYS\_3VSB.

If not use PECI, pin 27 28 could be configured as SMBus.

The trace between IT8758(Pin25) & oscillator (output) must Thicken and Shorten. In addition to that, the trace spacing must broaden.





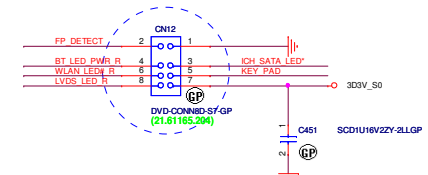
23 FP\_DETECT << FP\_DETECT

25 BT\_LED\_PWR\_CTRL << BT\_LED\_PWR\_CTRL

```
FP_DETECT H : FP not inserted (Internal Pull-High)
FP_DETECT L : FP inserted
```



SB-Lily requested.



## PWRBTN BUTTON with White LED









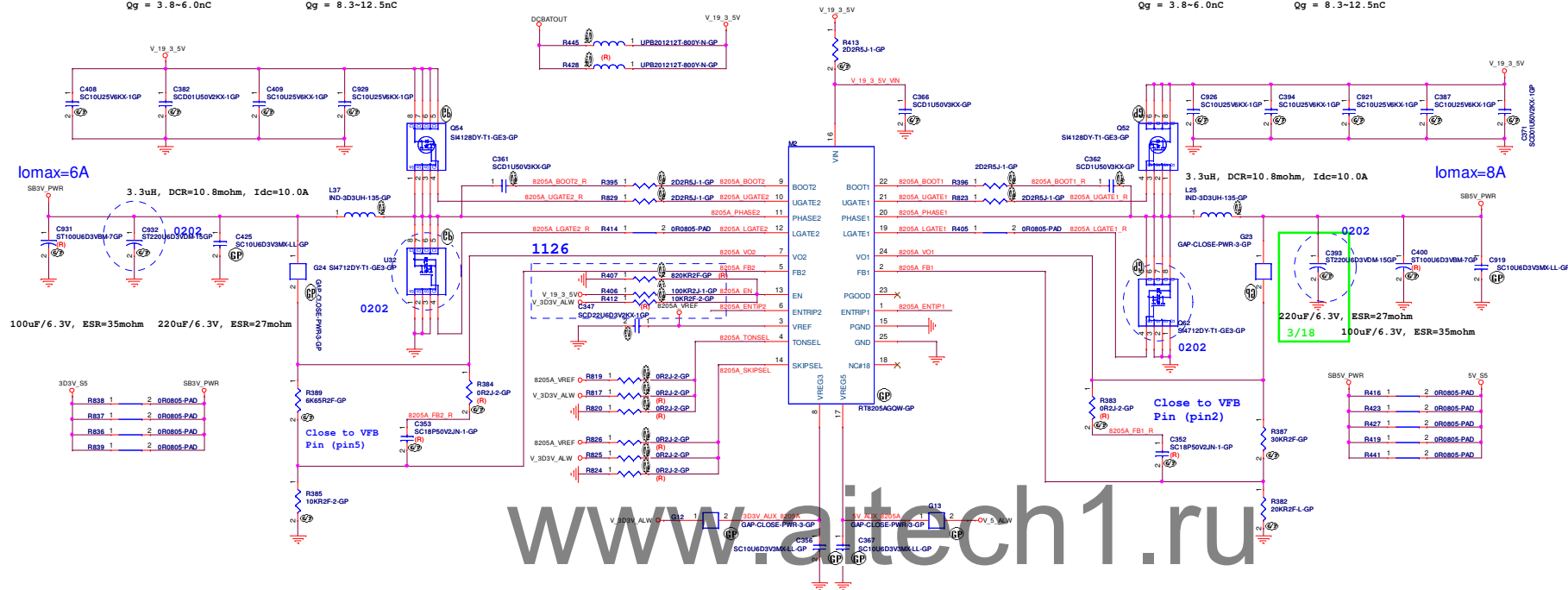
3/22



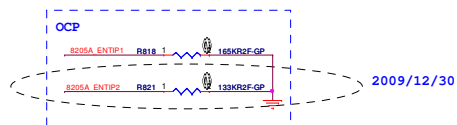


84.04128.037	SI4128DYP	84.04712.A37	SI4712DY
Vgs @ 4.5V,		Vgs @ 4.5V,	
Id = 6.0A,		Id = 8.2A,	
Rds(on) = 24.0~30.0mohm,		Rds(on) = 13.0~16.5mohm,	
Qg = 3.8~6.0nC		Qg = 8.3~12.5nC	

84.04128.037	SI4128DYP	84.04712.A37	SI4712DY
Vgs @ 4.5V,		Vgs @ 4.5V,	
Id = 6.0A,		Id = 8.2A,	
Rds(on) = 24.0~30.0mohm,		Rds(on) = 13.0~16.5mohm,	
Qg = 3.8~6.0nC		Qg = 8.3~12.5nC	



	GND	VREF	VREG3	VREG5
SKIPSEL	PWM	SKIP	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	330k/CH1 375k/CH2	400k/CH1 500k/CH2	400k/CH1 500k/CH2

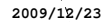




It might be cost down in SB.



11/16 Modify



11/02 Modify



IDmax = 0.75A  
For Mini-PCIE

11/02 Modify



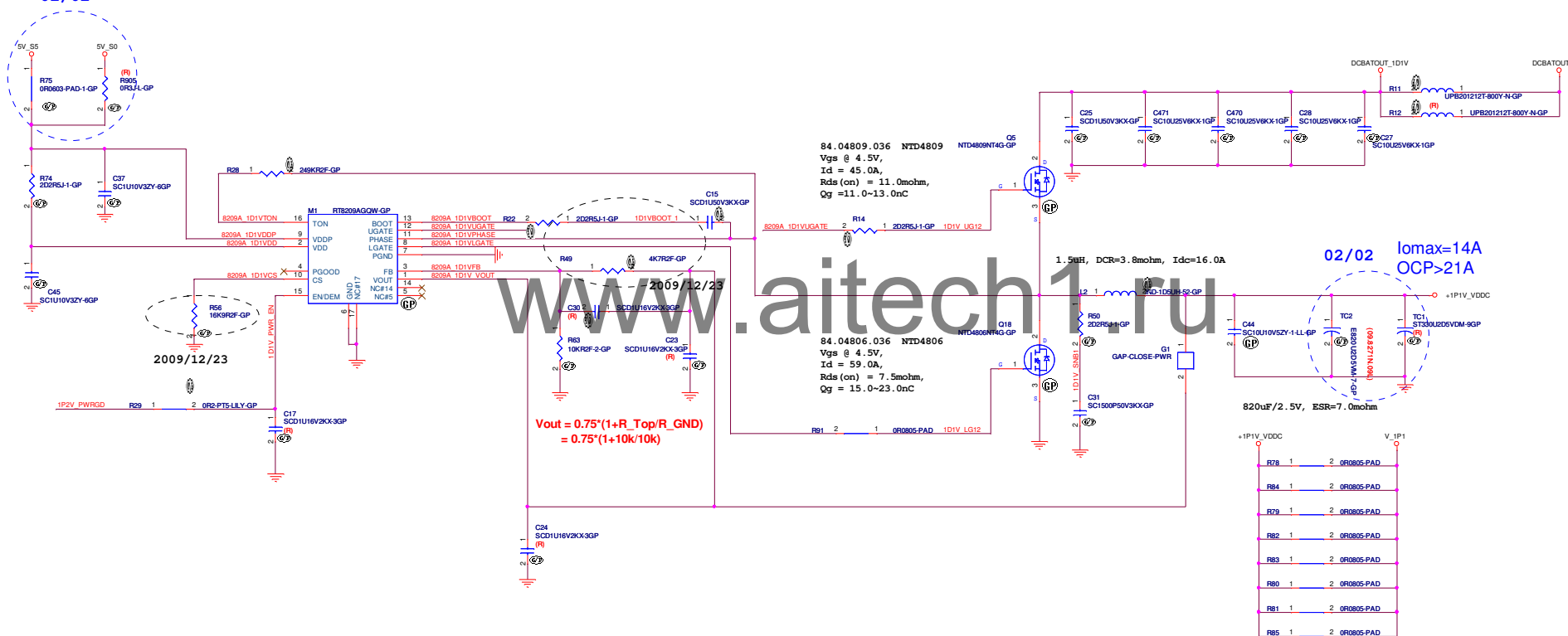
IDmax = 6A  
For USB



8.49 1P2V\_PWRGD >> 1P2V\_PWRGD

+1P1V\_VDDC(NB)

02/02

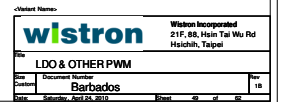
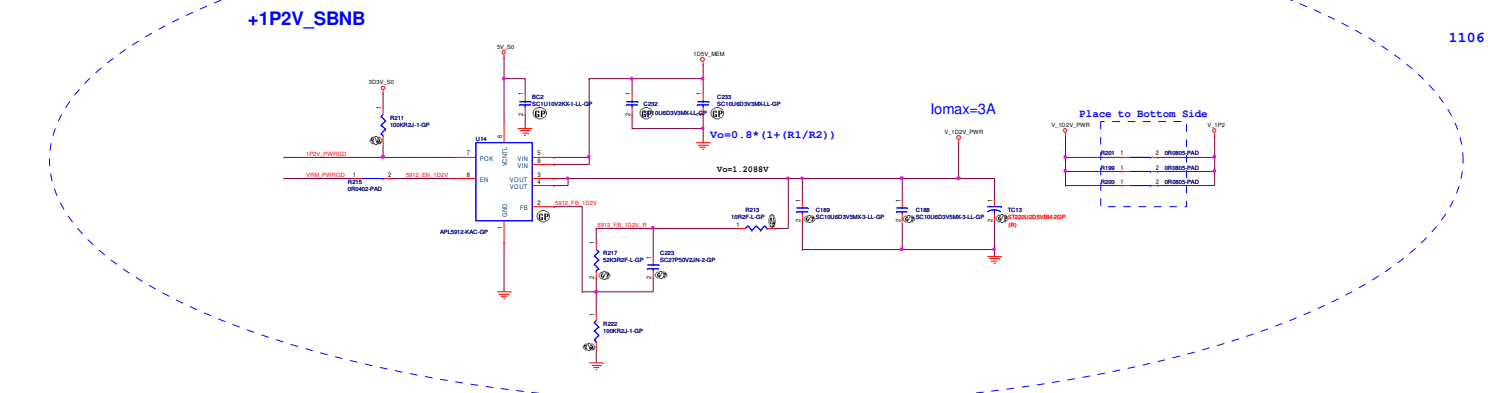


11/06









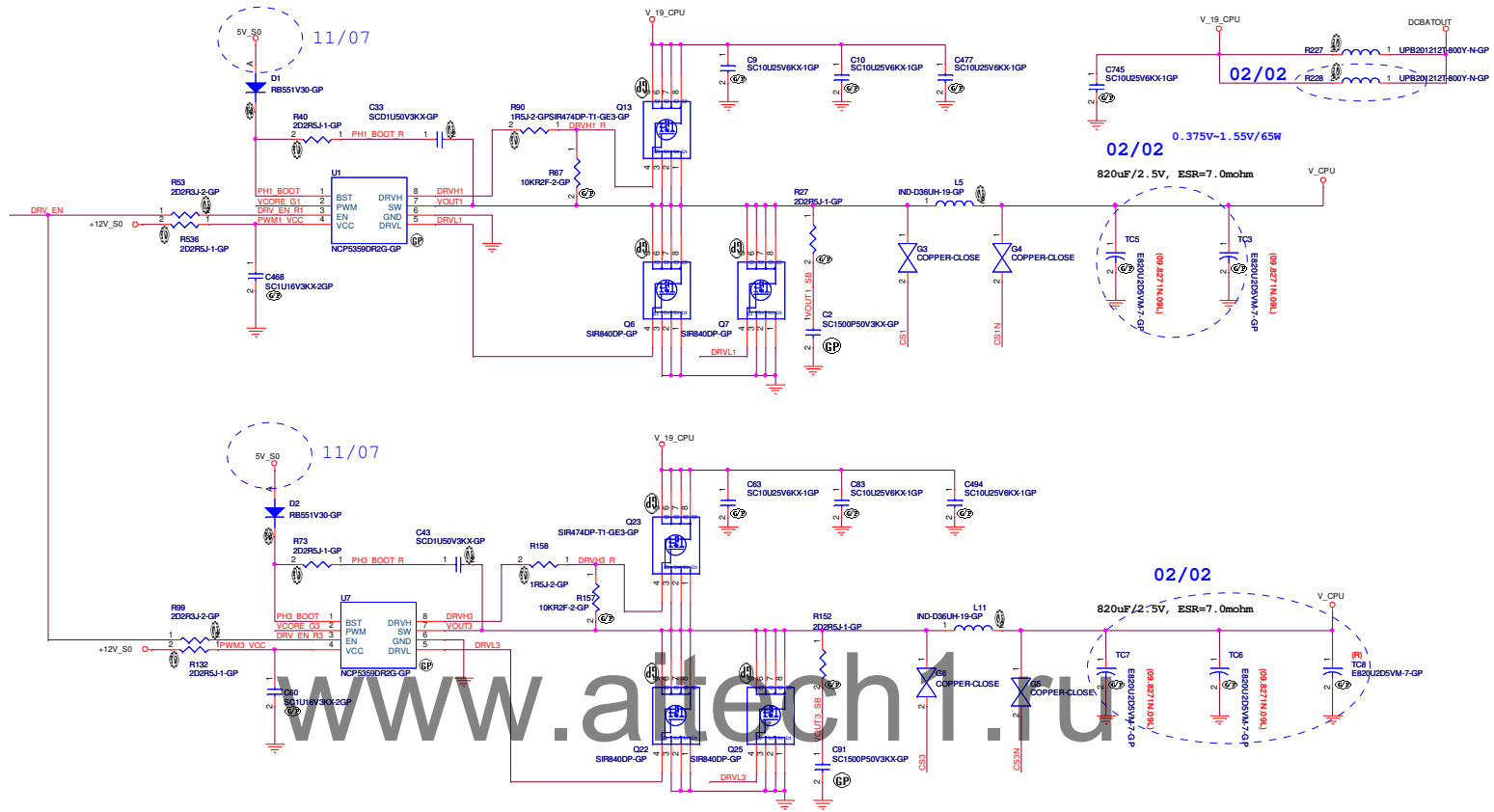






50 DRV\_EN >> DRV\_EN  
50 VCORE\_G1 >> VCORE\_G1  
50 CS1 >> CS1N  
50 CS1N >> CS1N

50 VCORE\_G3 >> VCORE\_G3  
50 CS3 >> CS3N  
50 CS3N >> CS3N

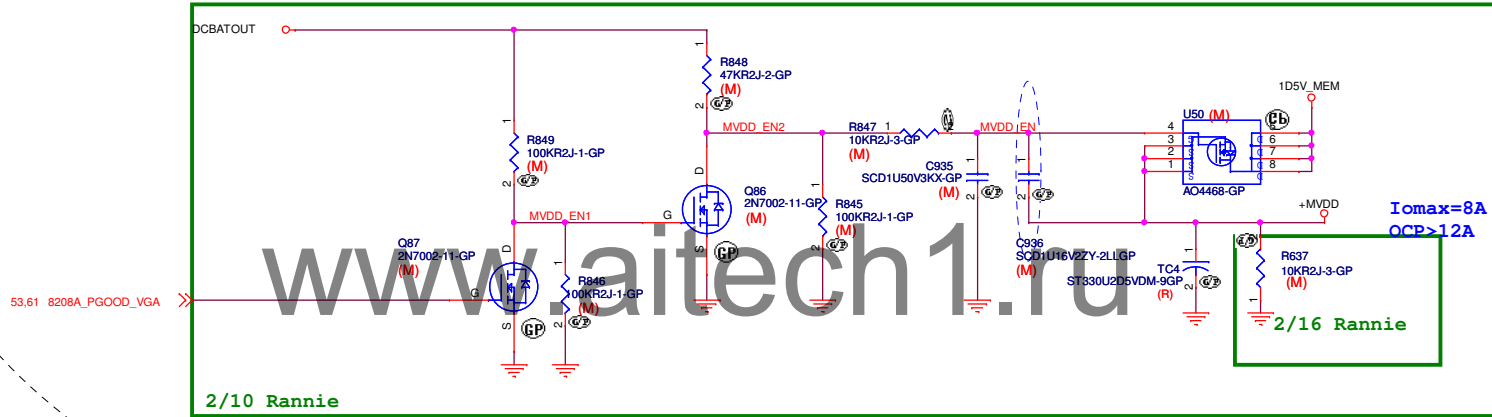


<Variant Name>

<b>wlstron</b>		Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title VCORE NCP5393 (2)			
Size C	Document Number Barbados		Rev 1B
Date: Saturday, April 24, 2010		Sheet 51 of 62	



2009/12/23



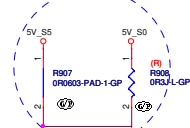
DIS / UMA

緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

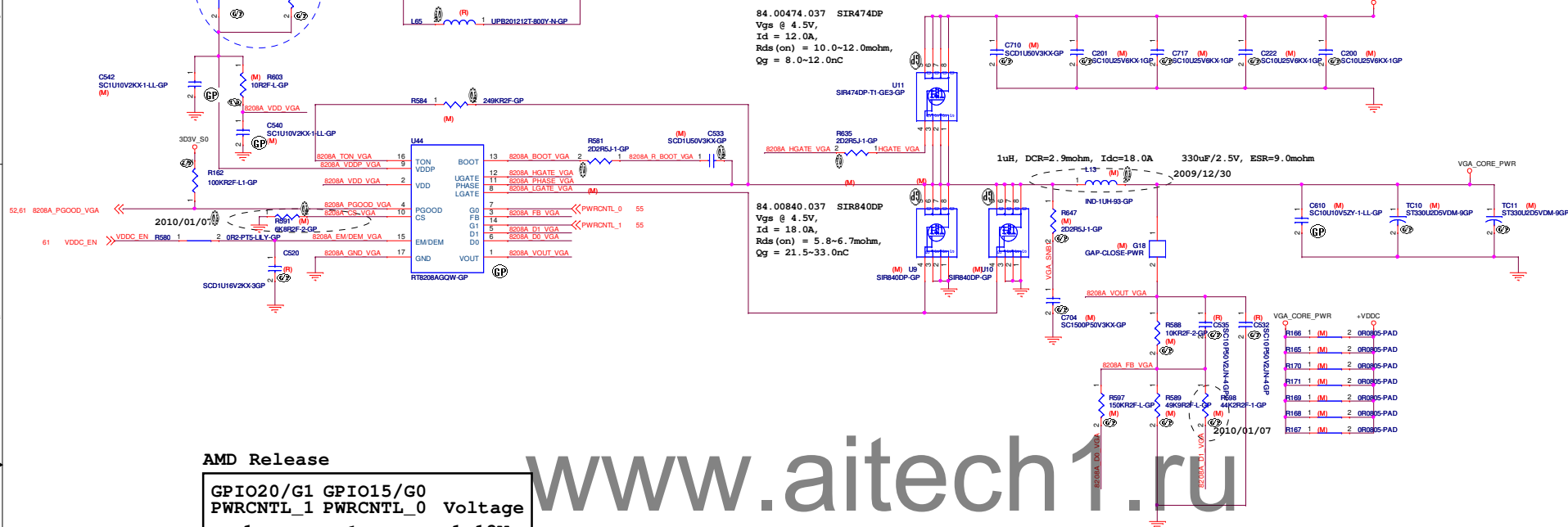
Title			RT8209E_1D5V_VRAM
Size	Document Number	Rev	
A3	JV71-TR8	1B	
Date: Saturday, April 24, 2010		Sheet	52 of 62



## RT8208A for VGA



**Iomax=16A, OCP>24A**



AMD Release

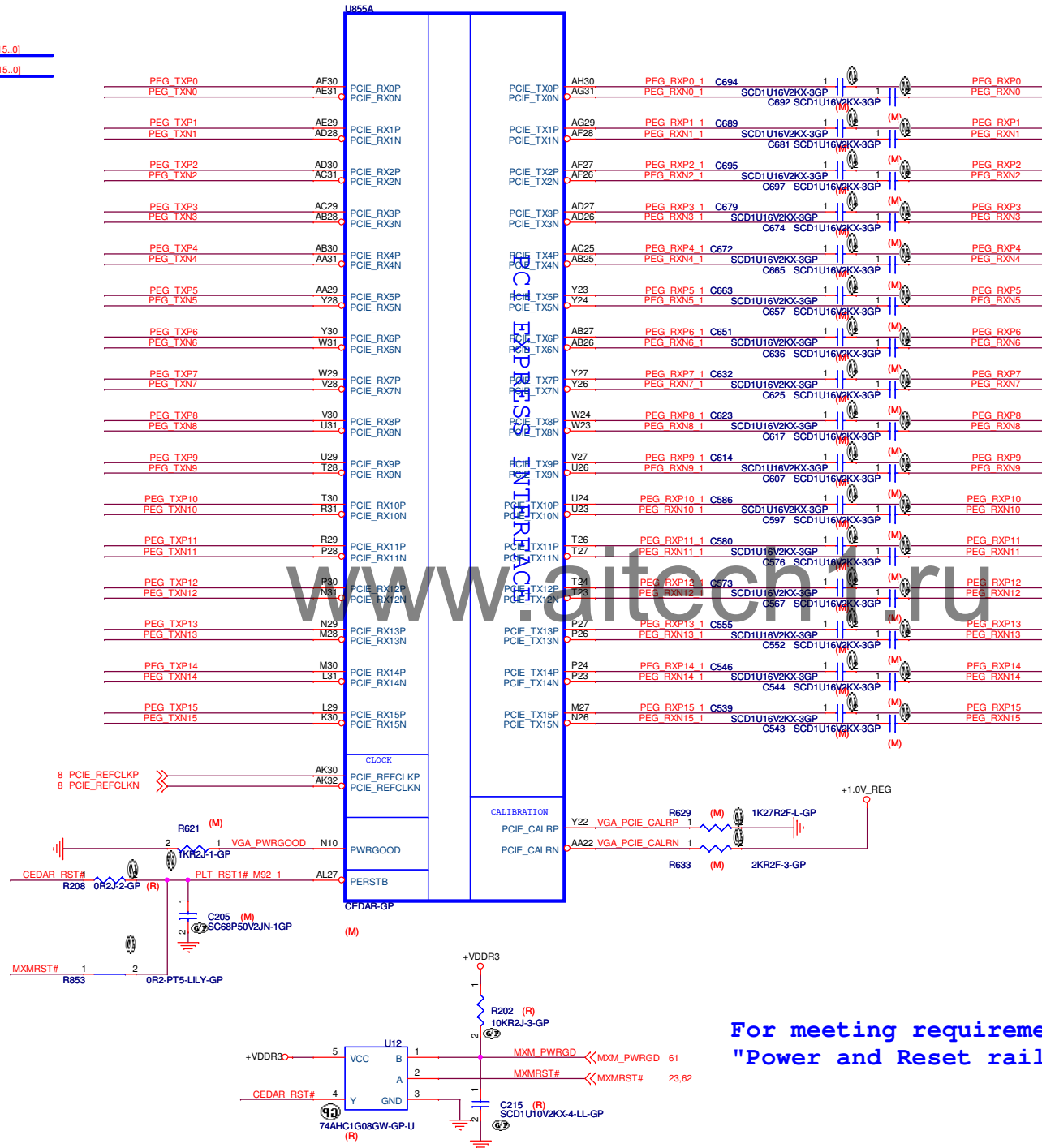
GPIO20/G1	GPIO15/G0	
PWRCNTL_1	PWRCNTL_0	Voltage
1	1	1.12V
1	0	1.07V
0	1	0.95V
0	0	0.9V

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16 PEG\_TXP[15.0] << PEG\_TXP[15.0]  
16 PEG\_TXN[15.0] << PEG\_TXN[15.0]

16 PEG\_RXP[15.0] << PEG\_RXP[15.0]  
16 PEG\_RXN[15.0] << PEG\_RXN[15.0]



Check!!

For meeting requirement of  
"Power and Reset rail up in 20ms"

DR / HMA

<p>緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>	
<p>Title Cedar PCIe</p>	
Size A3	Document Number B305
Date: Saturday, April 24, 2010	Sheet 54 of 62
<p>Rev 1B</p>	

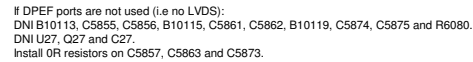






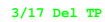








DIVIDER RESISTORS	GDDR5	GDDR3	DDR3
MVREF	1.5V	1.8/1.5V	1.5V
MVREF TO PWR	40.2R	40.2R	40.2R
MVREF TO GND	100R	100R	100R



## PIN STRAPS

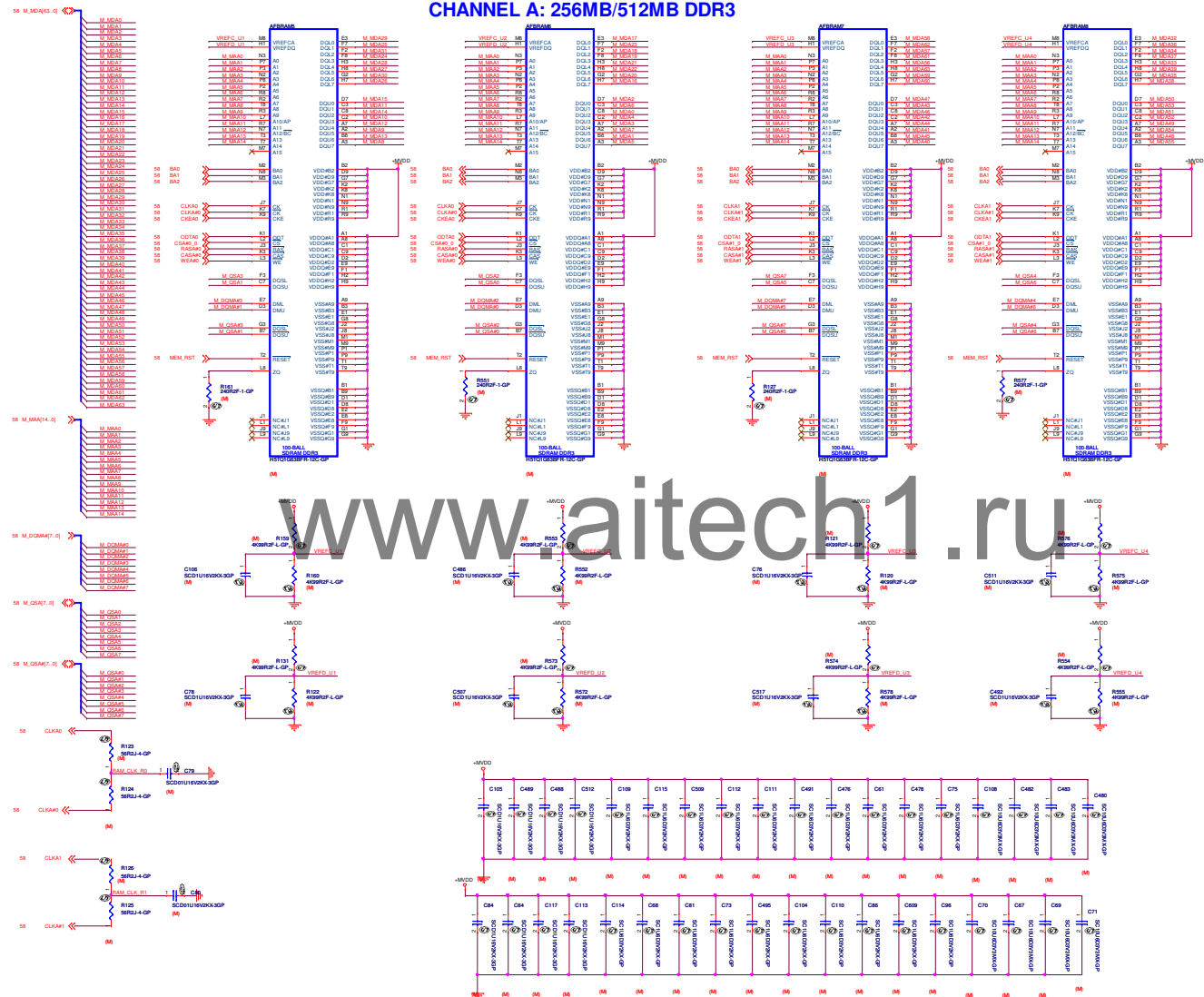


STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% TX output swing (Internal Pull-down) 1: Full TX output swing	GPIO0 and GPIO1 pulls up, need to be stuffed with G5556 if system board is controlling the PCIe swing. 1
TX_DEEMPH_EN	GPIO1	TX Transmitter De-emphasis Enable 0: Tx de-emphasis disabled (Internal Pull-down) 1: Tx de-emphasis enabled	1
BIF_GEN2_EN_A	GPIO2	PCIe Gen2 Enable 0: Advertises the PCIe device as 2.50GT/s capable at power-off (Internal Pull-down) 1: Advertises the PCIe device as 5.00GT/s capable at power-on	1
BIF_VGADIS	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	GPIO9 pull up needs to be stuffed with G5537 if system board is controlling the VGA capacity 0
ROMDCFG2[2]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO2 = 0, defines memory aperture size If GPIO2 = 1, defines ROM type 100: 128Mbit ROM2A (ST) 101: 1Mbit ROM1A (ST) 102: 128Mbit ROM2B (ST) 103: 2Mbit ROM2B (ST) 104: 4Mbit ROM2C (ST) 105: 1Mbit ROM2C (ST) 106: 512Mbit ROM2D12 (C/HP) 107: 1Mbit ROM2D12 (C/HP)	(Internal Pull-down) XXX
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	(Internal Pull-down) 0
AUD[1] AUD[0]	H5VNC V5VNC	00: No audio function 01: Audio for DP only 10: Audio for DP and HDMI display is detected 11: Audio for both DP and HDMI HDMI must only be enabled on systems that are legally certified. It is the responsibility of the system designer to ensure that the system is certified to support this feature.	XX
VP_DEVICE_STRAP_ENA	V5VNC	VP Device Strap Enable 0: Slave VP host port devices present 1: No slave VP host port devices reporting presence	(Internal Pull-down) 0
Reserved	H2VNC	Reserved  Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected, however, if it is connected to additional logic on the board, the logic must not allow this signal to be driven or pulled to any value except GND at reset.	0



```
72.51G63.C0U gDDRIII 64M*16 800MHz VRAM 54nm (Orion die) FBGA96P HYNIX H5TQ1G63BFR-12C
72.41164.H0U gDDR3 64M*16 800MHz VRAM E die FBGA 96P SAMSUNG K4W1G1646E-HC12
```

**CHANNEL A: 256MB/512MB DDR3**





Reserved  
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Taipei Hsien 221, Taiwan, R.O.C.

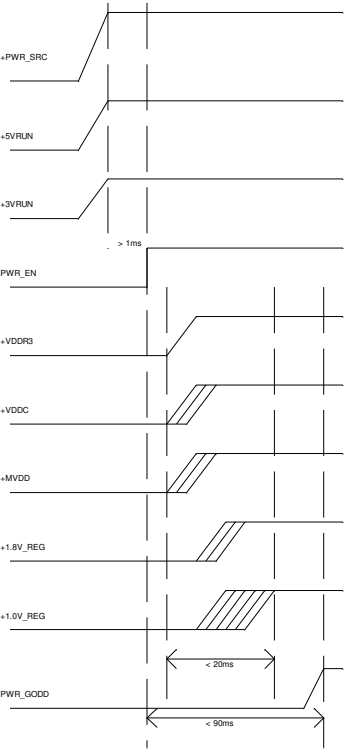
Title VRAM Rank 2 (Reserve)

Size A3	Document Number B305	Rev 1B
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Date: Saturday, April 24, 2010 Sheet 60 of 62



POWER UP SEQUENCE (not to scale)



VDDR3, A2VDD +VDDR3 should ramp before or simultaneously with +VDDC.  
+VDDC should ramp before +1.8V\_REG and +1.0V\_REG.

VDDC, VDDCI

VDDR1, MVDDQ/C

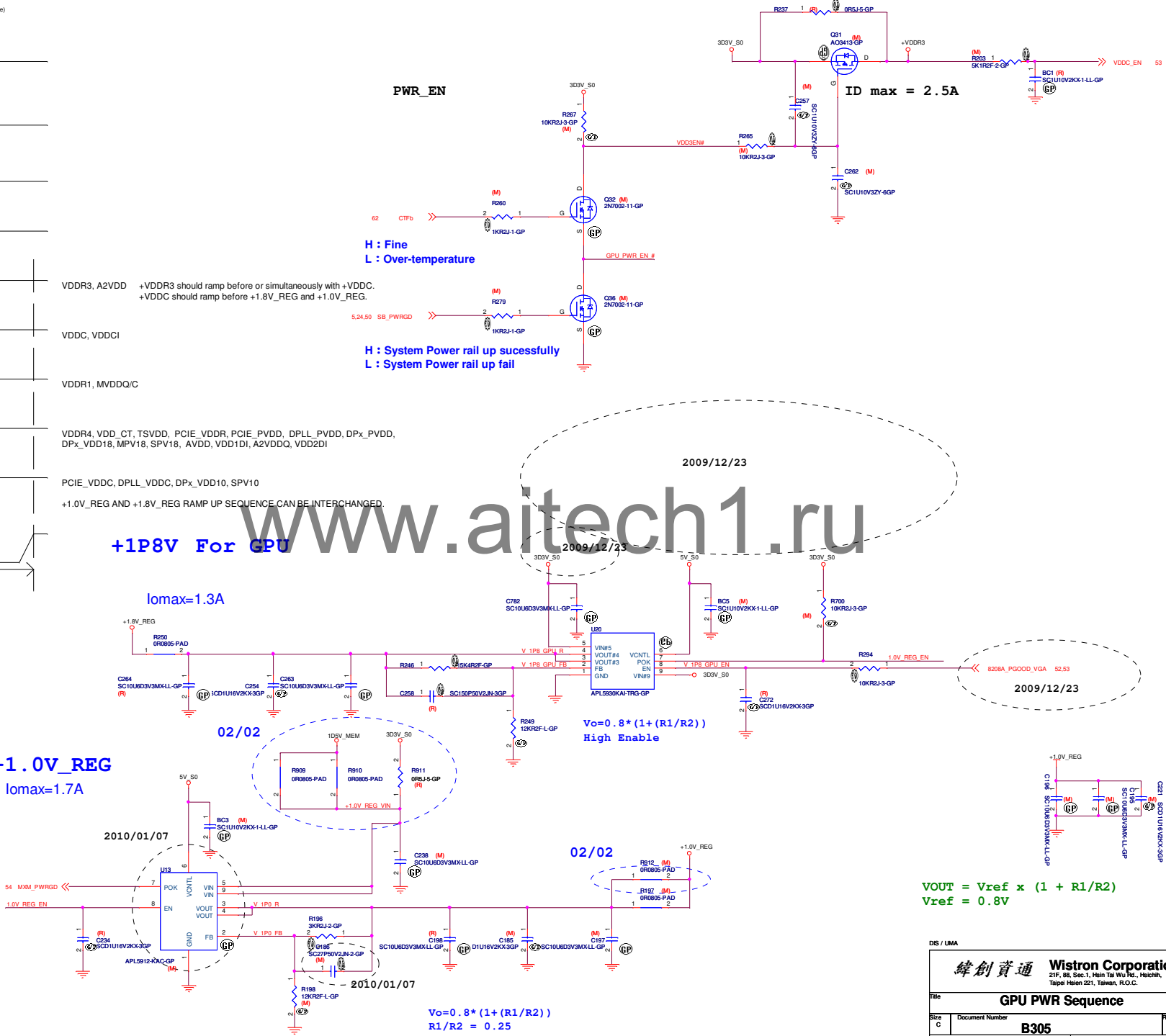
VDDR4, VDD\_CT, TSVDD, PCIE\_VDDR, PCIE\_PVDD, DPLL\_PVDD, DPX\_PVDD,  
DPX\_VDD18, MPV18, SPV18, AVDD, VDD1D1, A2VDDQ, VDD2D1

PCIE\_VDDC, DPLL\_VDDC, DPX\_VDD10, SPV10

+1.0V\_REG AND +1.8V\_REG RAMP UP SEQUENCE CAN BE INTERCHANGED.

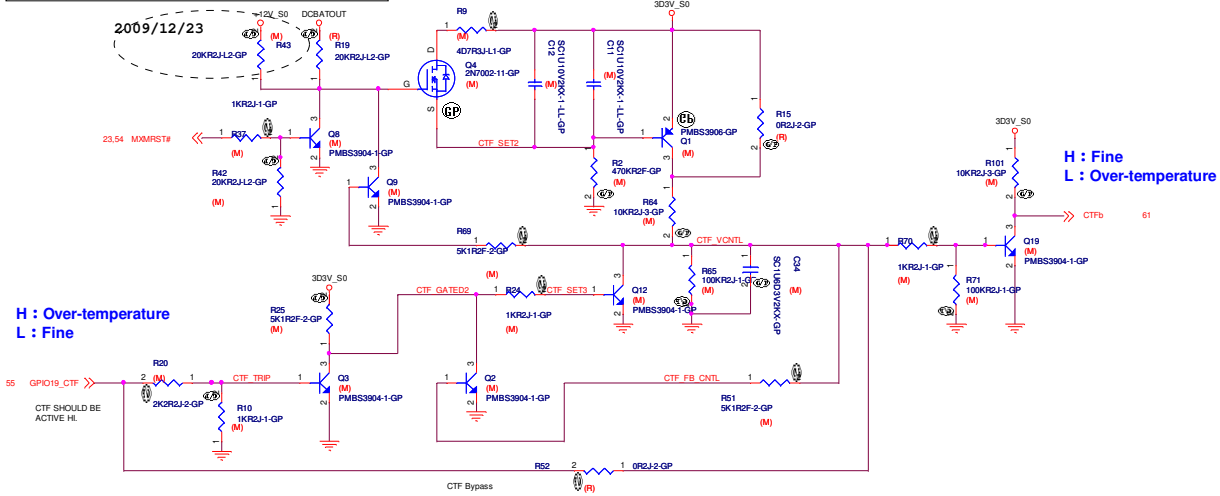
+1P8V For GPU

+1.0V\_REG  
Iomax=1.7A





## Critical Temperature Fault



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DIS / UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title	<b>CTF/PPLAY</b>
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Size C	Document Number <b>B305</b>	Rev <b>1B</b>
Date: Saturday, April 24, 2010      Sheet 62 of 62		